SOFTWARE DEFINED RADIO
USR SDR WORKSHOP, SEPTEMBER 2017
PROF. MARCELO SEGURA

SESSION 1: INTRODUCTION
• TUESDAY & FRIDAY,
• START TUESDAY 12, END TUESDAY 26
• LECTURES 4:30-6:15 PM
• COFFEE BREAK 15MIN
• HANDS ON LABS 6:30-8:00 PM
AGENDA

• SESSION 1:
  • INTRO TO SDR SYSTEMS
  • SDR AVAILABLE PLATFORMS
  • SOFTWARE TOOLS
  • LAB 1: INSTALLING B200 ON MATLAB

• SESSION 2:
  • AMPLITUDE MODULATION.
  • LAB 2: AM MODULATION AND DEMODULATION REAL TX/RX

• SESSION 3:
  • FREQUENCY & PHASE SYNCHRONIZATION
  • FREQUENCY MODULATION
  • LAB 3: IMPLEMENTING COHERENT RECEIVERS

• SESSION 4:
  • DIGITAL MODULATION
  • TIME & FREQUENCY SYNCHRONIZATION
  • LAB 4: FM TX/RX

• SESSION 5:
  • QPSK MODULATION
  • LAB 5: FREQ & TIME SYNC
  • LAB 6: REAL TIME QPSK.
“It is a type of radio where PHY layer can be changed by software”

- Antenna
- RX Filter/LNA
- TX PA
- Duplexer

- AD/DA conversion
- Up/down frequency conversion
- Filtering/resampling

MATLAB/SIMULINK
1992: Joe Mitola publish a paper where he mention for the first time the concept of “Software Radio”

1996: The fist SDR forum was created.

1998: A start up called Vanu Inc, was the first company that start working with SDR for cellular application.

2001: Eric Blossom start developing GNURadio

2003: Ettus Research offer the first series of USRP

2006: TI & Xilinx joint forces to develop embedded SDR evaluation kits.

2008: First Open BTS GSM project.

2011: A graphical interface is developed for GNURadio, called GRC, GNURadio Companion. Matlab start giving support for USRP boards.

2012: Amarisoft develop the first NodoB for LTE Cellular communications.

2013: Ettus sales low cost SDR called B200
SDR...FOR WHAT?

- Fast and flexible communication prototypes.
- Research new protocols.
- Helps to understand the basis of communication system. Great tool for teaching.
- Considering the broad bandwidth it is possible to implement comm system on not usual frequency bands.
- Scientific, Industrial and Academic applications.
WHAT IS SDR...... IS THIS??

Base band Radio
WHAT IS SDR...... MAY BE THIS??

Full Digital (Zero IF) Radio
WHAT IS SDR…… OK THIS!!!
WHICH PARAMETER CAN I TUNE?

**Diagram:**

- **Rafael Micro R820T Silicon Tuner**
  - RF Image Rejection Filter
  - IF Lowpass Filter
  - Low Noise RF Amplifier
  - Active Gain Control
  - RF VCO controlled with a fractional PLL

- **RTL2832U – Digital IF to Baseband Receiver functionality**
  - In Phase
  - Quadrature Phase
  - Resampler / synch.
  - Decimation Filtering

**Parameters over IFC serial bus**

**Radio Frequencies (RF) → Intermediate Frequencies (IF) → Baseband**

- LO - Local Oscillator
- NCO - Numerically Controlled Oscillator
- PLL - Phase Locked Loop
- RF - Radio Frequency
- VCO - Voltage Controlled Oscillator

- $f_{LO}$ - frequency synthesised by RF VCO
- $f_{sA}$ - sampling rate of ADC (28.8MHz)
- $f_i$ - intermediate frequency
- $f_o$ - frequency of output IQ samples (up to 2.8MHz)
- $K$ - gain of RF amplifiers
- $n$ - discrete sample index
RTL-SDR RX EXAMPLE

- Digital
  - Decimation Filtering
  - Resampler / synch.
  - RF Antenna & input to MATLAB and Simulink

- Analogue
  - Anti-alias Filter
  - IF Lowpass Filter
  - RF Image Rejection Filter
  - Active Gain Control

Signal Power (dBm)

- Baseband
  - $f_s = 2.8$ MHz

- Digitised IF
  - $f_{IF}
  - $f_{IF}/2
  - $f_{IF}/2$

- RF
  - $f_{RF}$

- $f_{adc}$
  - 28.8 MHz

Parameters:
- $f_{vco}$ - frequency synthesised by RF VCO
- $f_{sam}$ - sampling rate of ADC (28.8 MHz)
- $f_{if}$ - intermediate frequency
- $f_{IQ}$ - frequency of output IQ samples (up to 2.8 MHz)
- $g$ - gain of RF amplifiers
- $n$ - discrete sample index
WHAT IS THE FRONT-END?

- It is the interconnection between Antenna & ADC.
- It has to transform from Analog-Digital and DA.
- The ADC/DAC can be included or not.
- Principal task:
  - Up/down conversion.
  - Frequency translation, mixer IF.
  - Power amplification, LNA, AGC.
  - Filtering.
- Is the heart of any SDR, depending on his capabilities it will be the flexibility of the SDR.
- The parameter are programed using a driver that can run locally (FPGA/CPU) or in a external host.
COMMON CHARACTERISTICS

- Frequency range: from near DC up to Ghz.
- Number of ADC/DAC bits. Resolution.
- Dynamic Range.
- Instantaneous Bandwidth. (condition the transfer speed ADC/DAC)
- Full duplex or half duplex. MIMO.
- Power
- Usually not mentioned on Datasheet:
  - Imbalance on IQ
  - Phase Noise
  - Noise Figure
COMMON CHARACTERISTICS

- Typically considering 16 bits/sample, 32 bits/sample (IQ).
- USB:
  - 2.0 @480Mbps -> 15MSps (8Mhz)
  - 3.0 @3.2Gbps -> 100MSps (56Mhz)
  - Example: USRP B200 USB 3.0
- Ethernet:
  - GigE @ 1Gbps -> 31.25MSps (20Mhz)
  - 10 GigE @ 10Gbs -> 312.5MSps (200Mhz)
- PCIe:
  - Gen 3 @ 8 Gbps/line. Low latency, higher bandwidth.
COMMERCIAL FRONT-ENDS

- **AD9361**
  - RF Agile Transceiver™
  - 70 MHz – 6000 MHz Tuning range
  - 200kHz – 56 MHz RF channel Bandwidth

- **ADP1755**
  - Low $V_{in}$ / $V_{out}$ LDO

- **ADP2164**
  - Synchronous, step-down dc-to-dc regulator

- **M24C02**
  - EEPROM

- **AD7291**
  - 8-channel, SAR ADC
  - Housekeeping

- **40 MHz Crystal**
AD9361: 2 Rx + 2 Tx

AD9364: 1 Rx + 1 Tx

Major sections:
- RF input/output paths
- RF PLL/LO (70 – 6000 MHz)
- BB fractional N synthesizer
- Clock generation
- ADC/DAC
- Digital filters
- Digital interface
- Enable state machine
- RX Gain (AGC)
- TX Attenuation
- Aux DAC/ADC and GPOs
- Analog and Digital Correction/Calibration
INITIAL CALIBRATION

Initialization Calibrations
- BBPLL VCO Calibration
- RF Synthesizer Charge Pump Calibration
- RF Synthesizer VCO calibration
- Baseband RX Analog Filter Calibration
- Baseband TX Analog Filter Calibration
- Baseband TX Secondary Filter
- RX TIA Calibration Equations
- RX ADC Setup
- Baseband DC Offset Calibration
- RF DC Offset Calibration
- RX Quadrature Calibration
- TX Quadrature Calibration

Factory Calibrations
- Internal DCXO
- TX RSSI (TX Monitor)
- RX RSSI
- RX GM / LNA Gain Step Calibration
- TX Power Out Vs TX Attenuation and TX Power Out Vs Carrier Frequency
Each filter stage results in some unique amplitude rolloff and group delay in the passband.

Problem:
- How to understand each filter stage effect on:
  - Amplitude rolloff in passband
  - Group delay in passband
- How to design a FIR filter that compensates for effects from previous stages?

-3dB point defines “bandwidth”, but still not flat from DC to half of “bandwidth”
MULTI STAGE FILTER

- AD9361 analog filters in Tx and Rx chains
- SINC Filter effects from ADC/DAC
- Digital Half Band interpolators & decimators

- FIR design for filtering, equalization and optional additional interpolation & decimation
AGC

- Gain is variable in all stages
- Two separate but identical receive paths
- Slow attack
- Fast attack

- Each Rx has own programmable HW gain table and index pointers.
- Pointer moves up and down the table, which changes the gain in one or more of the blocks shown left.
- Full Table and Split Table mode
EVOLUTION

AD9361

3G/4G picocell, SDR, point-to-point, satcom, IoT aggregator

3G/4G femtocell, UAV, wireless surveillance

3G/4G macro BTS, massive MIMO, SDR

3G/4G small cell BTS, massive MIMO

100mm

62mm

133mm

50.95mm

68mm

26.4mm

EPIQ SOLUTIONS
Sidekiq

USRP E310

DR ING MARCELO SEGURA

USC SDR WORKSHOP
<table>
<thead>
<tr>
<th>Feature</th>
<th>LMS6002D</th>
<th>LMS7002M</th>
<th>LMS8001+</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radio Spectrum</td>
<td>300MHz – 3.8GHz</td>
<td>100kHz – 3.8GHz</td>
<td>100kHz – 12GHz</td>
</tr>
<tr>
<td>RF Bandwidth</td>
<td>28 MHz</td>
<td>120 MHz (through analog ports) 60 MHz (through digital interface)</td>
<td>120 MHz</td>
</tr>
<tr>
<td>TRX Configuration</td>
<td>SISO</td>
<td>MIMO</td>
<td>MIMO</td>
</tr>
<tr>
<td>Duplex</td>
<td>Full</td>
<td>Full and half</td>
<td>Full and half</td>
</tr>
<tr>
<td>Sample Rate (ADC/DAC)</td>
<td>40 Mspss</td>
<td>160/640 Mspss</td>
<td>160/640 Mspss</td>
</tr>
<tr>
<td>Digital Gates</td>
<td>50K</td>
<td>1M</td>
<td>1M</td>
</tr>
<tr>
<td>Integrated MCU</td>
<td>no</td>
<td>yes</td>
<td>no</td>
</tr>
<tr>
<td>Power consumption (W)</td>
<td>1.5</td>
<td>1</td>
<td>1.5</td>
</tr>
<tr>
<td>Availability</td>
<td>Jan 2011</td>
<td>October 2014</td>
<td>To be announced</td>
</tr>
</tbody>
</table>
CPU, GPU, FPGA, DSP, ASIC??

• TRADE OFF:
  • General propose vs Application specific
  • Complexity vs Performance
  • Power consumption vs Performance

• FPGA, is useful because of it capacity of parallel processing.

• FPGA great flexibility with embedded CPU.

• DSP are statics and usually complex programming.

• FPGA allow to implement hardware co-processors for intensive task like FFT o coders
FPGA

- Simple schematic

- Now SDR manufactures are moving GPP to FPGA: Embedded.

- How to program FPGA:
  1. Define the logic.
  2. Codify using Verilog or VHDL.
  3. Synthesize and create the bit stream (UHD)
  4. Load the bit stream on FPGA.
  5. Run the software application on the embedded CPU.
The best of two words: sequential & parallel

2 ARM 32 bits @ 1.3Ghz (PS)

FPGA (PL).

Interfaces: USB, ETH, SPI

How to split the code to get the best performance??
FRONT END + FPGA

PROCESSING UNIT

Zynq All Programmable SoC

Front end + FPGA

Dual ARM A9

USC SDR WORKSHOP
HOW TO CHOOSE AN SDR?

• Depending on the application.

• Restrictions: size, power, bandwidth, latency, budget, time, performance.

• It has any sense to build my own SDR... USC-SDR ??