USC Viterbi
School of Engineering
Center for Cyber-Physical Systems and the Internet of Things

SOFTWARE DEFINED RADIO

USR SDR WORKSHOP, SEPTEMBER 2017

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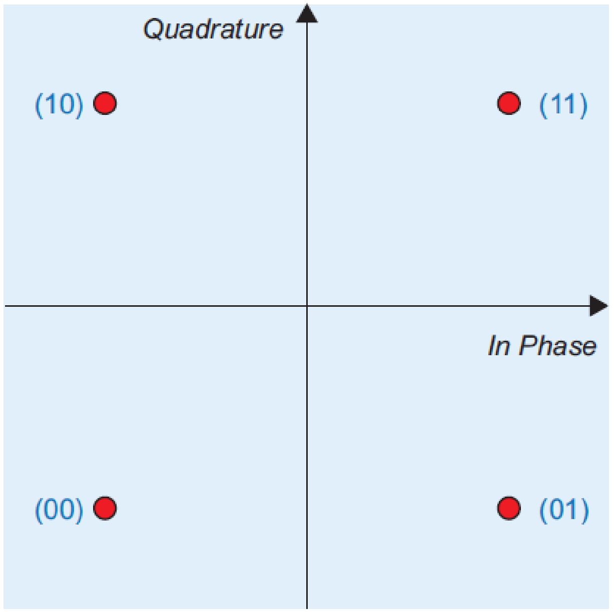
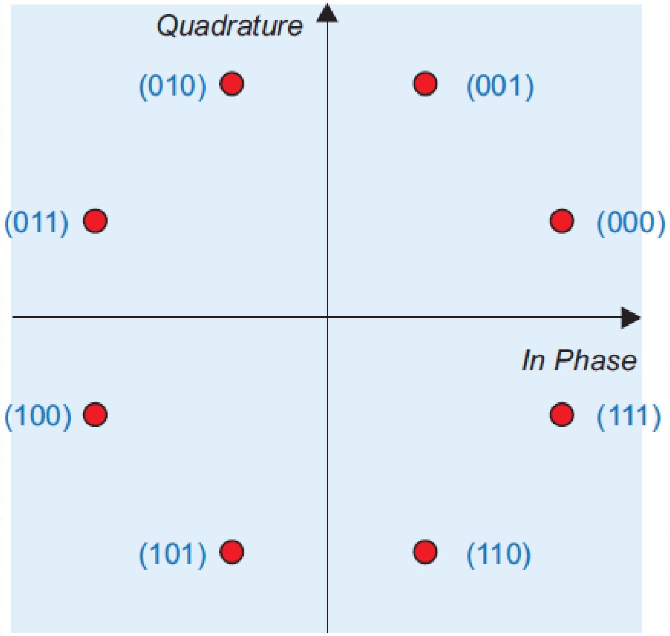
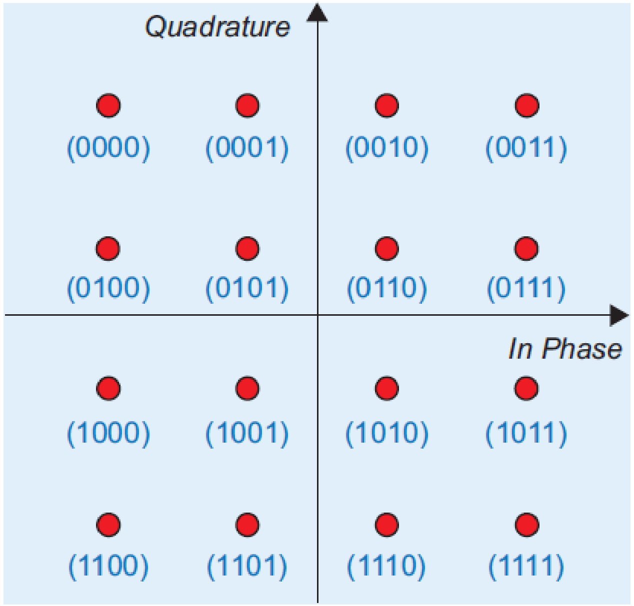
SESSION 4: DIGITAL MODULATION

BIT TO SYMBOLS MAPPING

- QPSK y QAM, using Gray code to minimize BER.



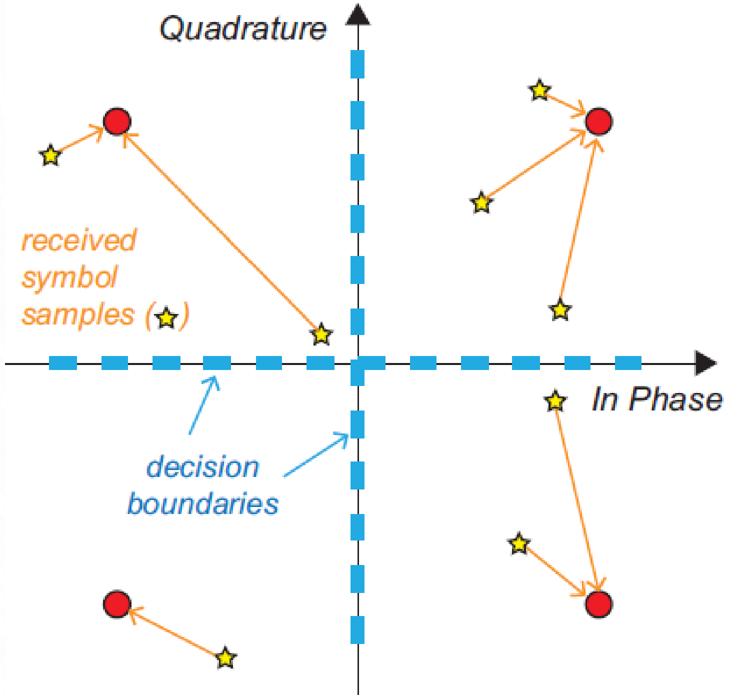




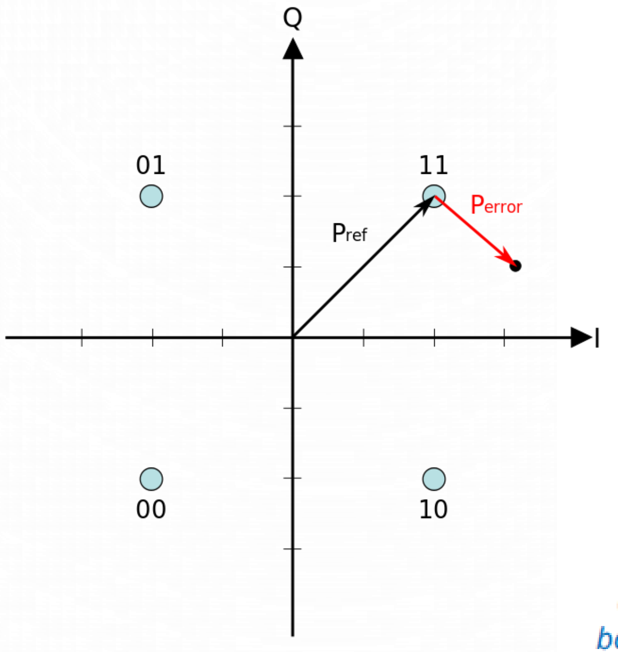
(b) **16-QAM**

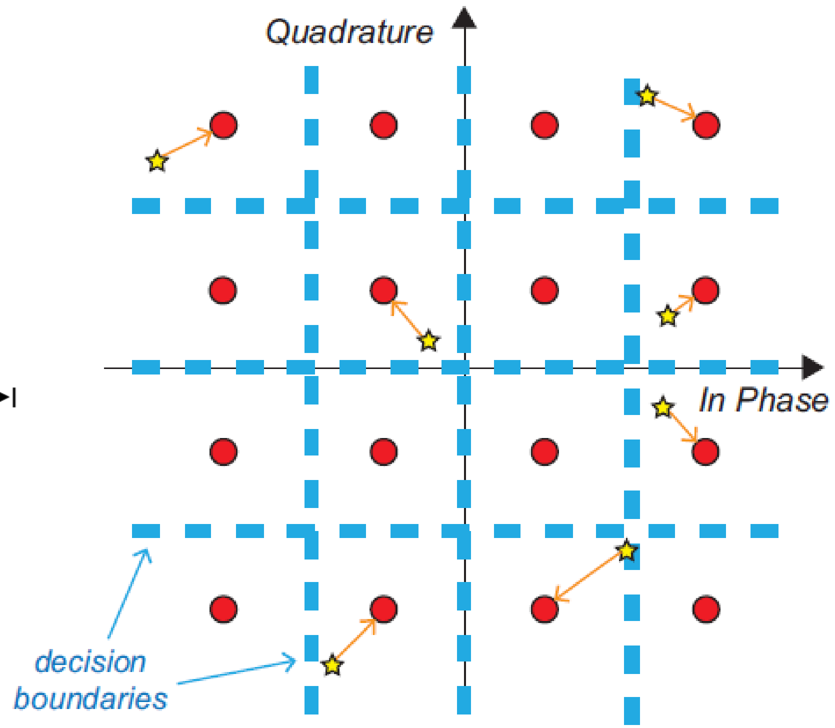
DE-MAPPING

- Compare with boundary regions. Measure the EVM.



(a) **4-QAM / QPSK**



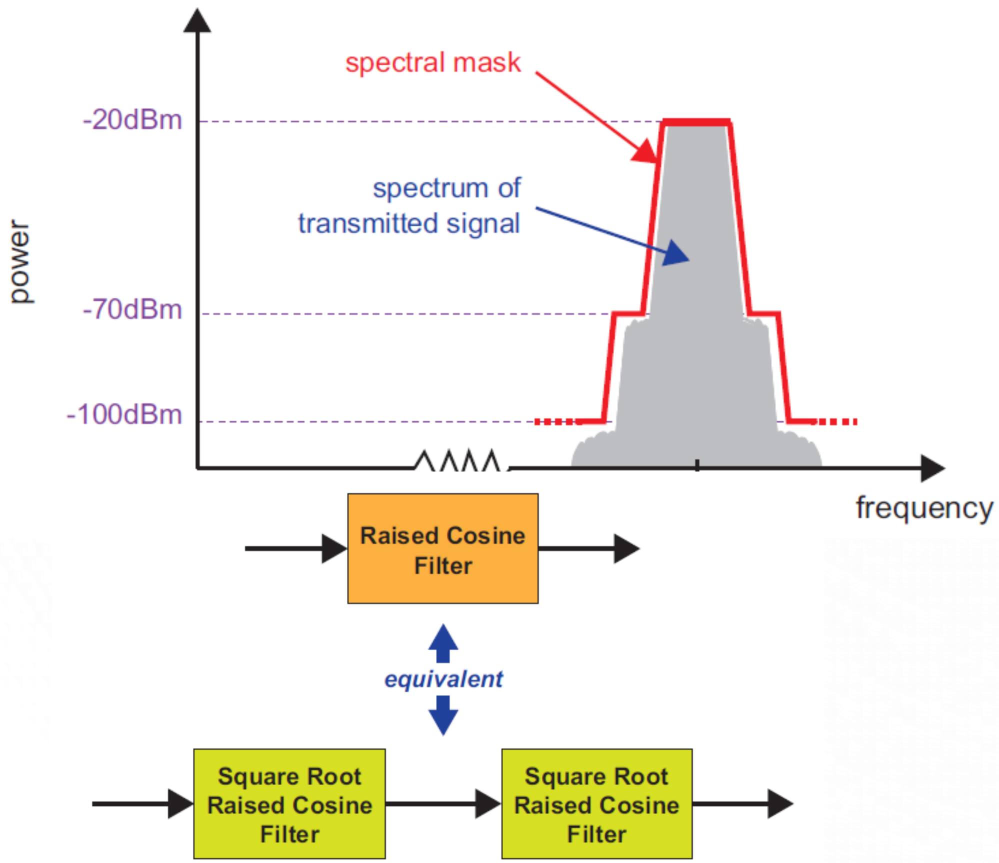


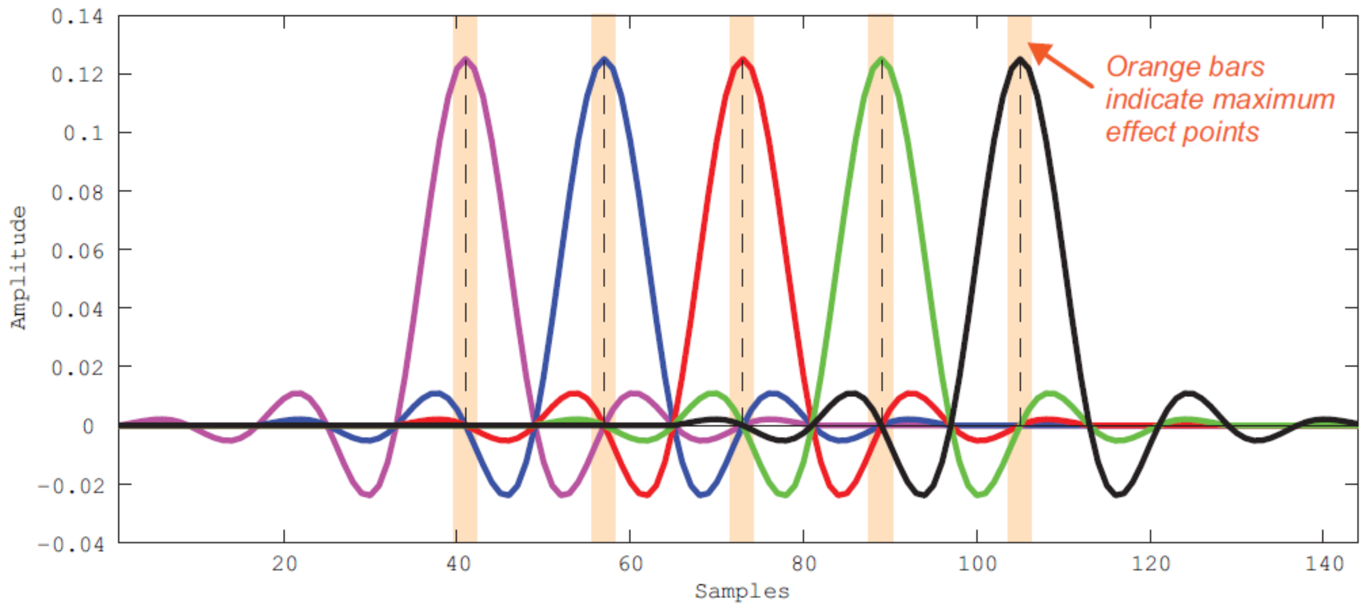
(b) **16-QAM**

$$\mathrm{EVM(dB)} = 10\log_{10}\left(\frac{P_{\mathrm{error}}}{P_{\mathrm{reference}}}\right) \qquad \mathrm{EVM}(\%) = \sqrt{\frac{P_{\mathrm{error}}}{P_{\mathrm{reference}}}} \times 100\%$$

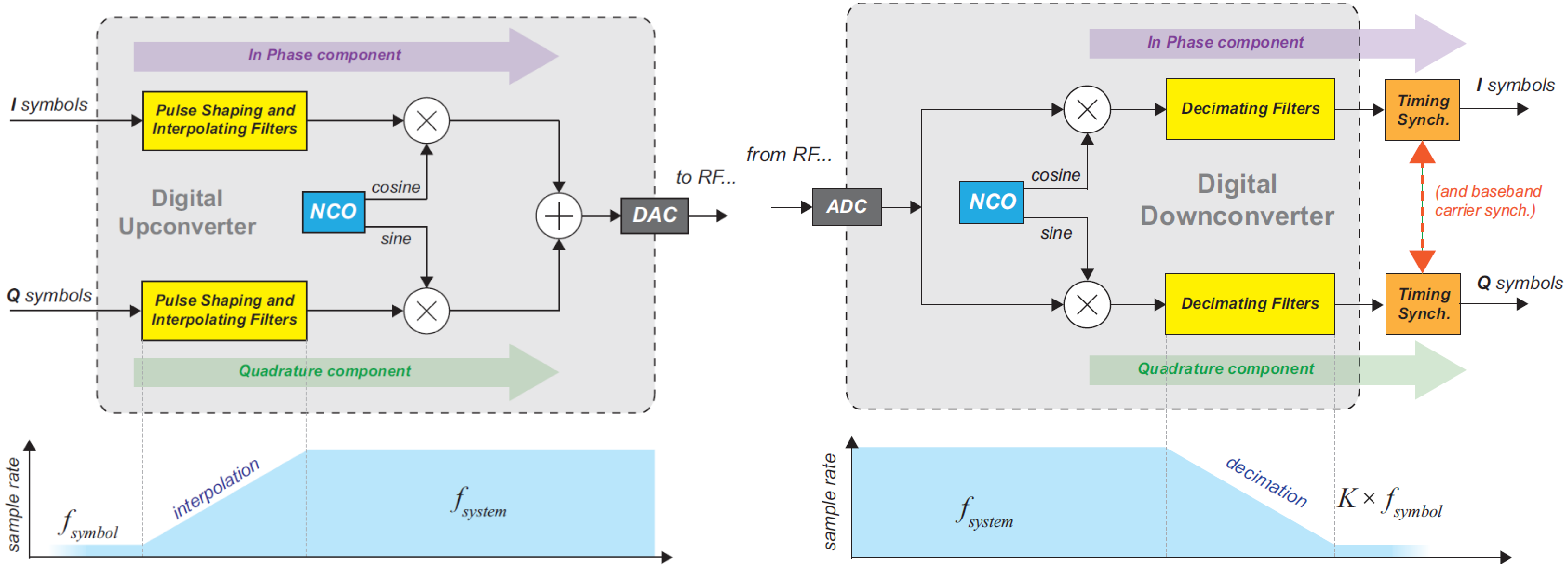
PULSE SHAPING (RRC)

- The tx/rx Match has the main objective to limit the bandwidth and reduce the ISI.
- The most common used Match filter is the Raised Cosine, because of its Zero-ISI property. With TX/RX RRC filter we get the equivalent RC.





MULTIRATE FILTERS ON FPGA

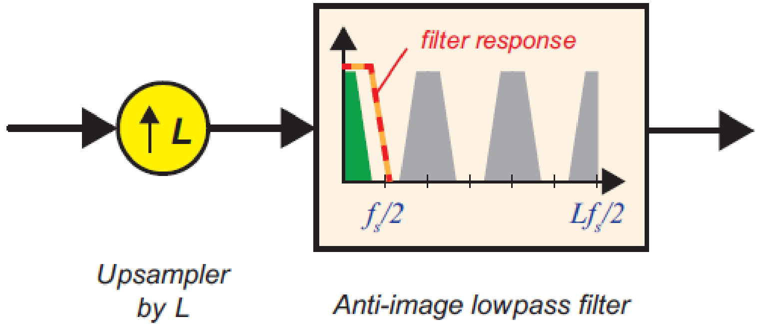


MULTIRATE FILTERS ON FPGA

- Used to interpolate and decimate.
- Up-sampling: spectral images are generated at multiples of the original sampling rate, so we need to remove them.

Interpolator= upsampling +

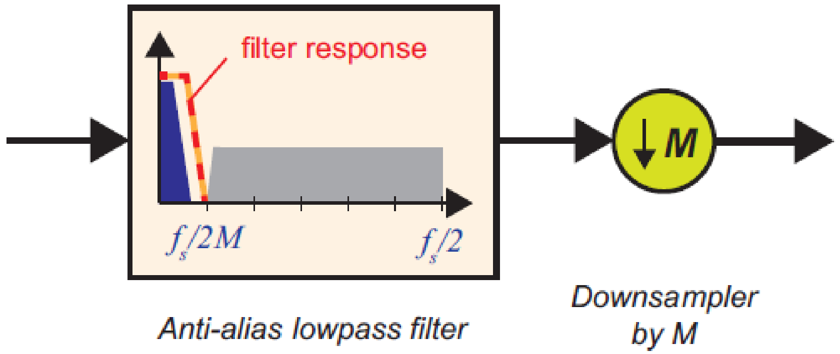
low pass filter (anti-image)



Down-sampling: the filter has to limit the out-of-band components in order to avoid aliasing after downsampling.

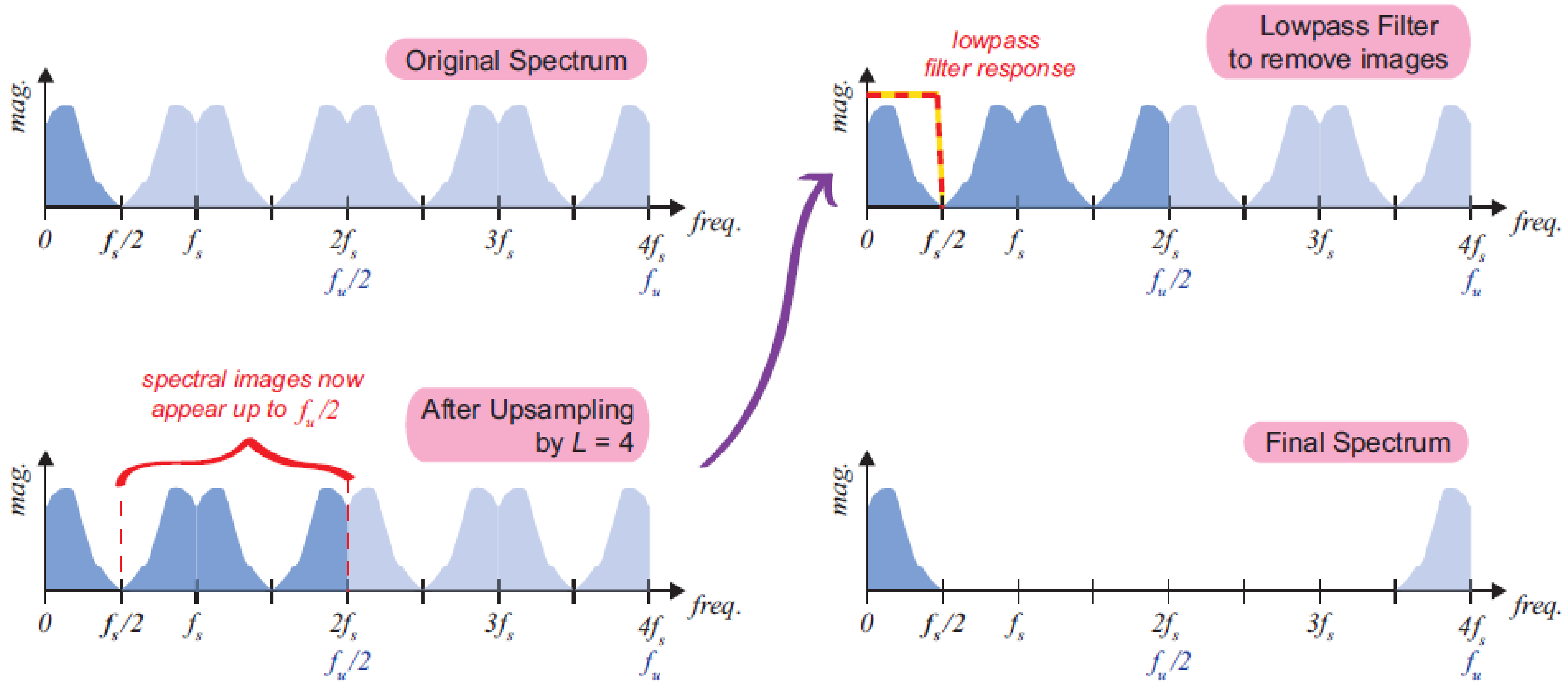
Decimation = low pass filter (Anti-Alias)

+ downsampling



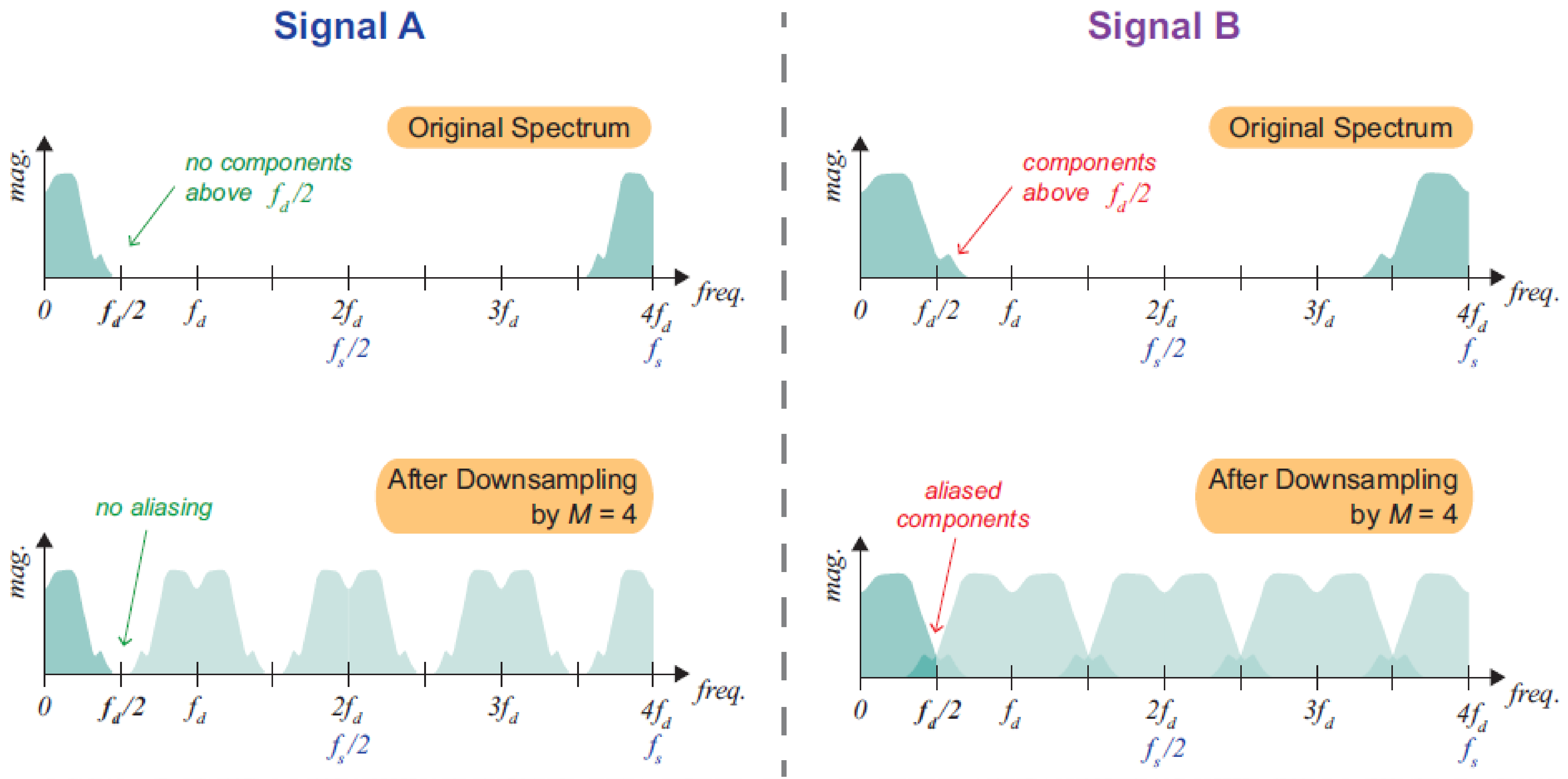
MULTIRATE FILTERS ON FPGA

- INTERPOLATOR



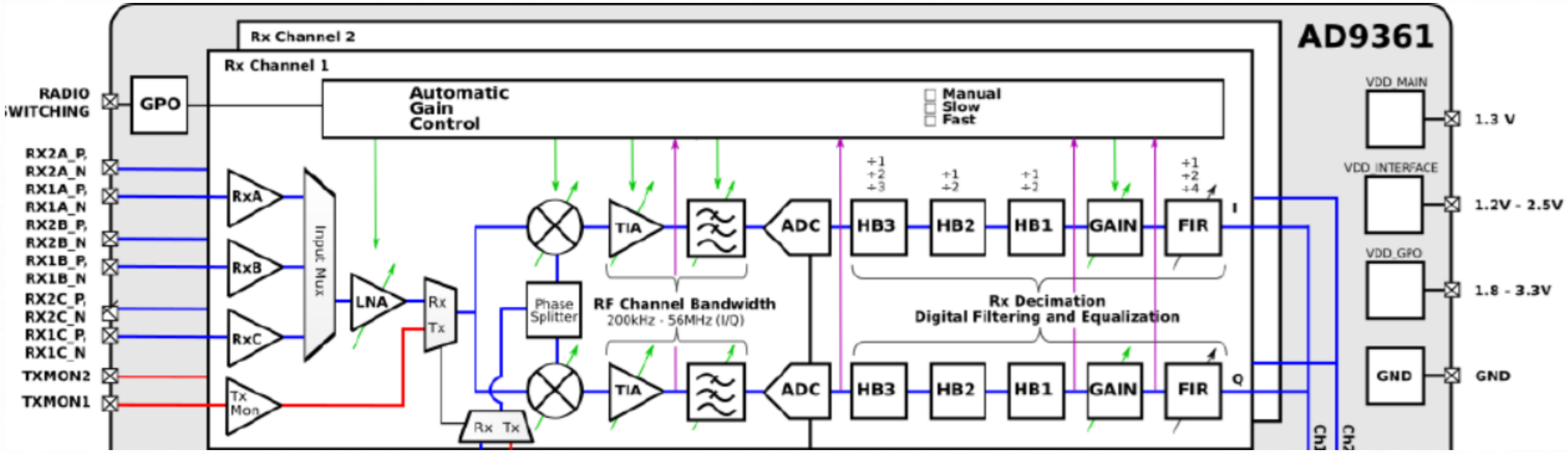
MULTIRATE FILTERS ON FPGA

- DECIMATOR



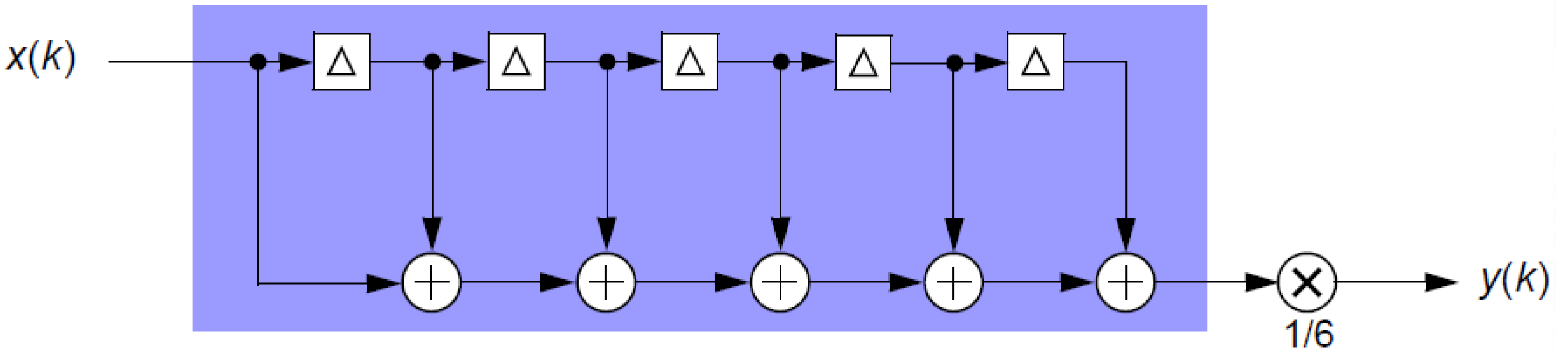
EFFICIENT FILTERS

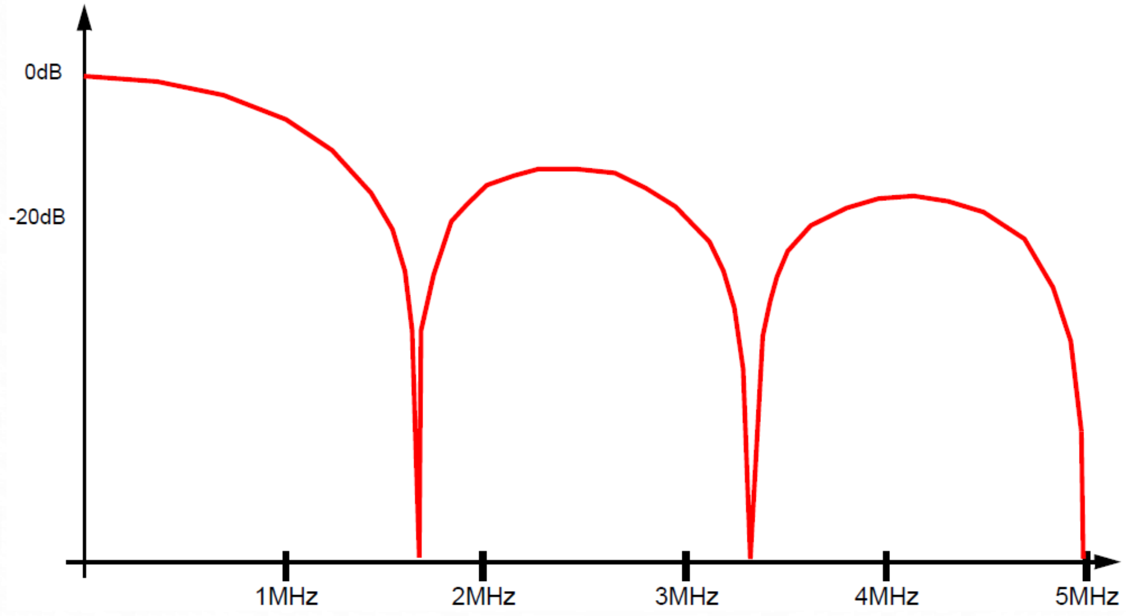
- Usually, DDC and DUC are implemented with a cascade of computationally efficient filters. This is really important on hardware implementations like FPGA or in SDR front-ends.
- Moving average.
- Integrator.
- Differentiator
- Combiner
- CIC filters



MOVING AVERAGE

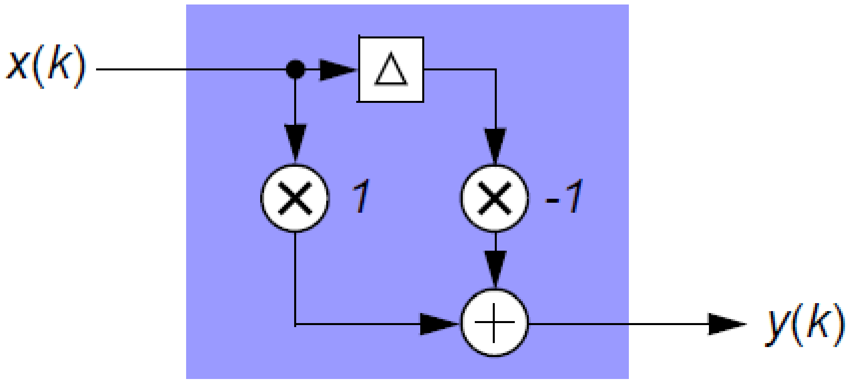
- Is the simplest **Low Pass** filter. All filter coefficients are set to '1'.
- Low cost, not multipliers.
- N/2 spectral notched on 0-Fs/2
- Ex: Fs=10Mhz

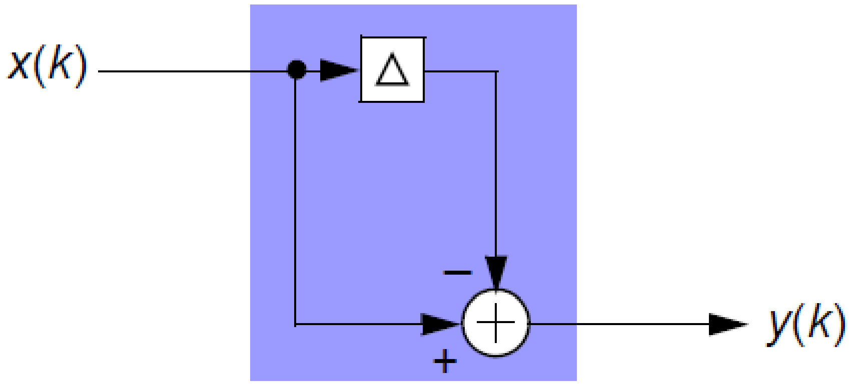




DIFFERENTIATOR

- Two weight filter with +1 and -1 coefficient.

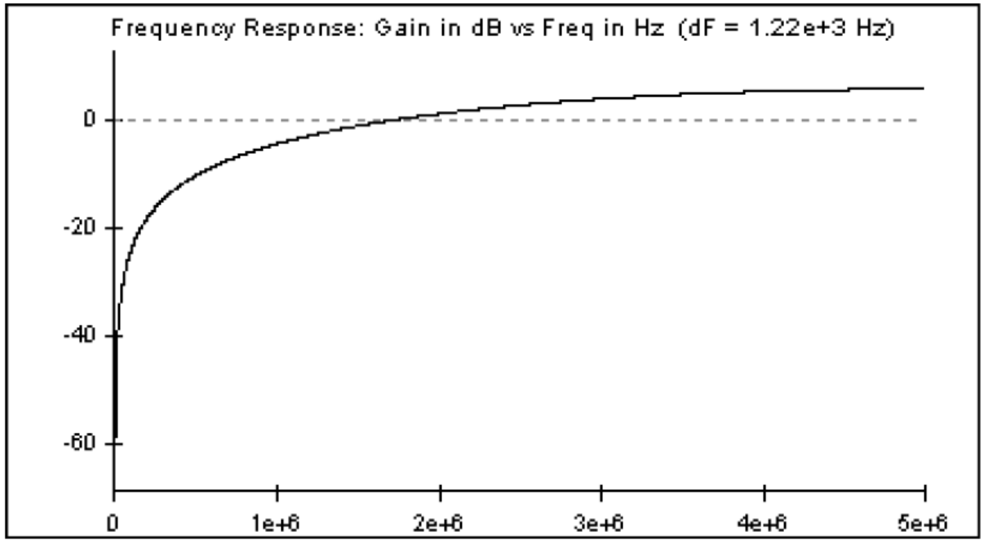




- Is the simplest **High Pass** filter.

$$Y(z) = X(z) - X(z)z^{-1}$$

$$H(z) = \frac{Y(z)}{X(z)} = 1 - z^{-1}$$

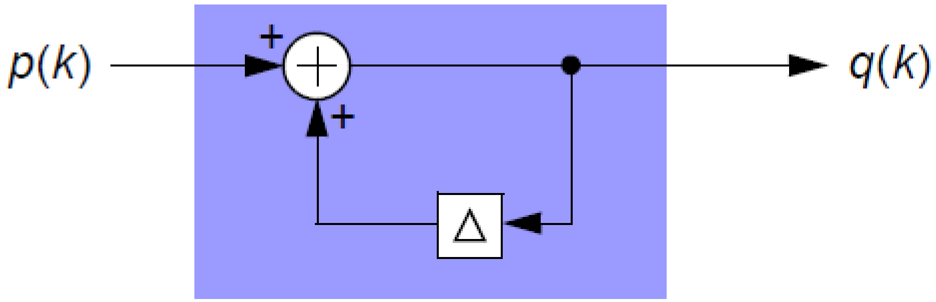


INTEGRATOR

- Essentially a simple weight IIR.
- It is a Low Pass, with no multipliers.
- Infinite gain at DC

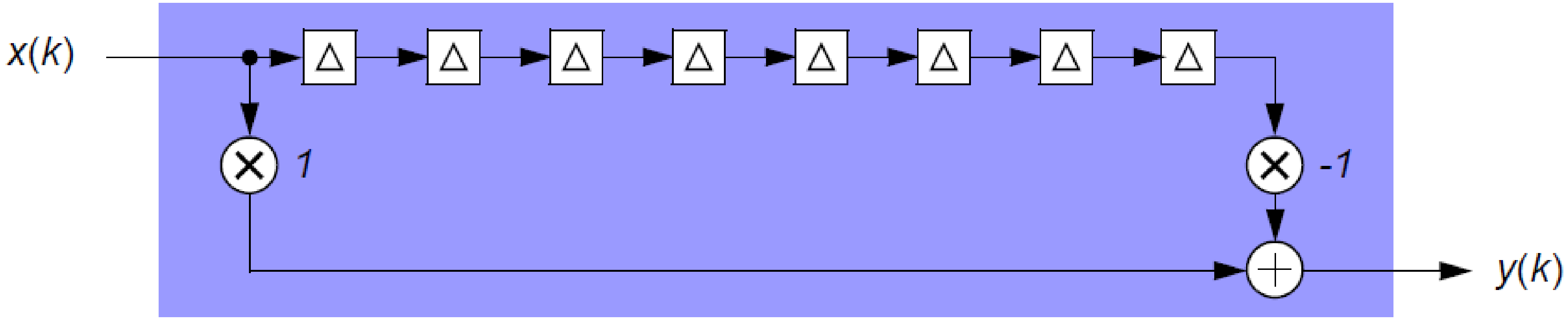
$$Q(z) = P(z) + Q(z-1)$$

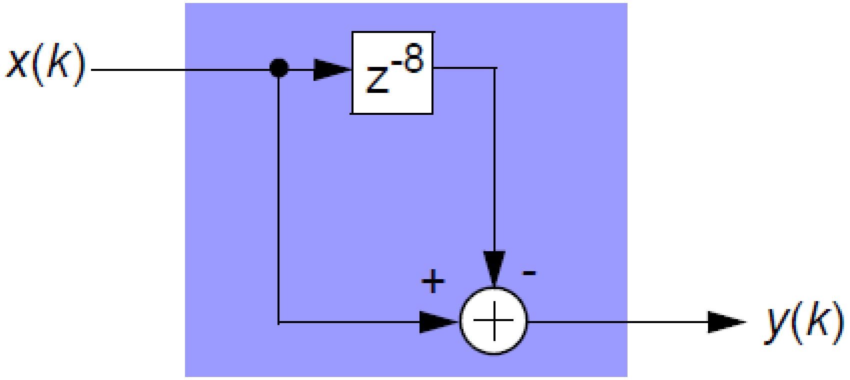
$$G(z) = \frac{Q(z)}{P(z)} = \frac{1}{1 - z^{-1}}$$

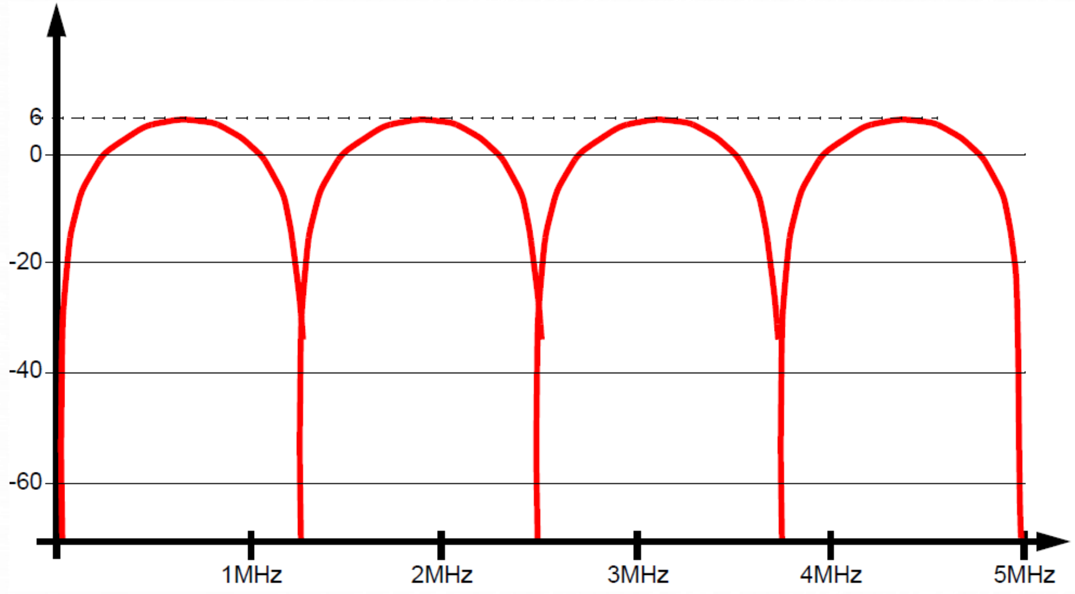


COMBINER FILTER

- Weight =1 and -1 at the extremes
- N/2 spectral zeros
- No multipliers required.

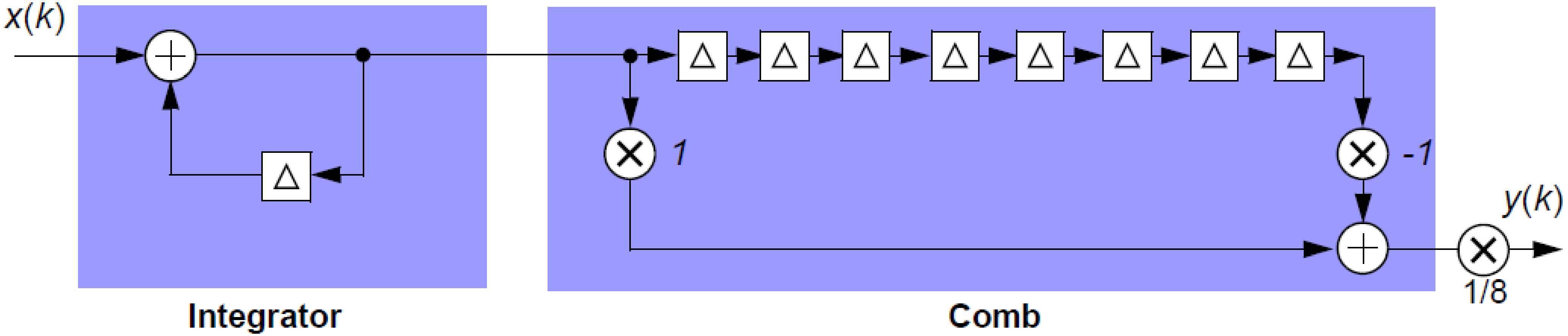






INTEGRATOR-COMB FILTER

- IC structure are used to implement MA filter.
- Advantages: require only two adders vs 8 adders on MA
- Disadvantages: require more delay elements (FF are cheap on FPGA)

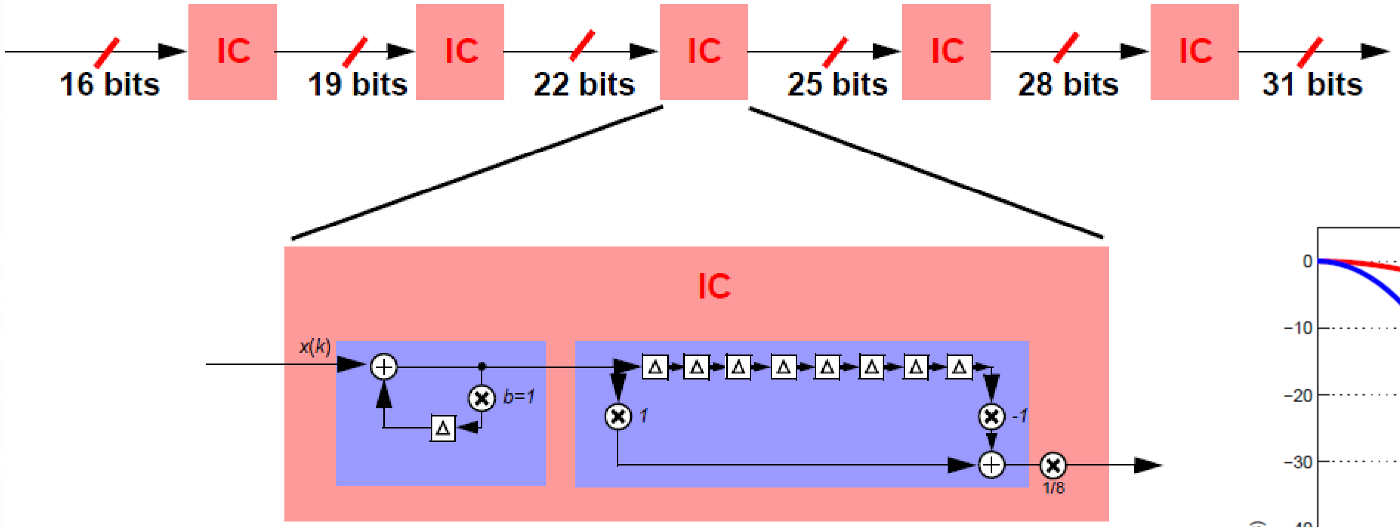


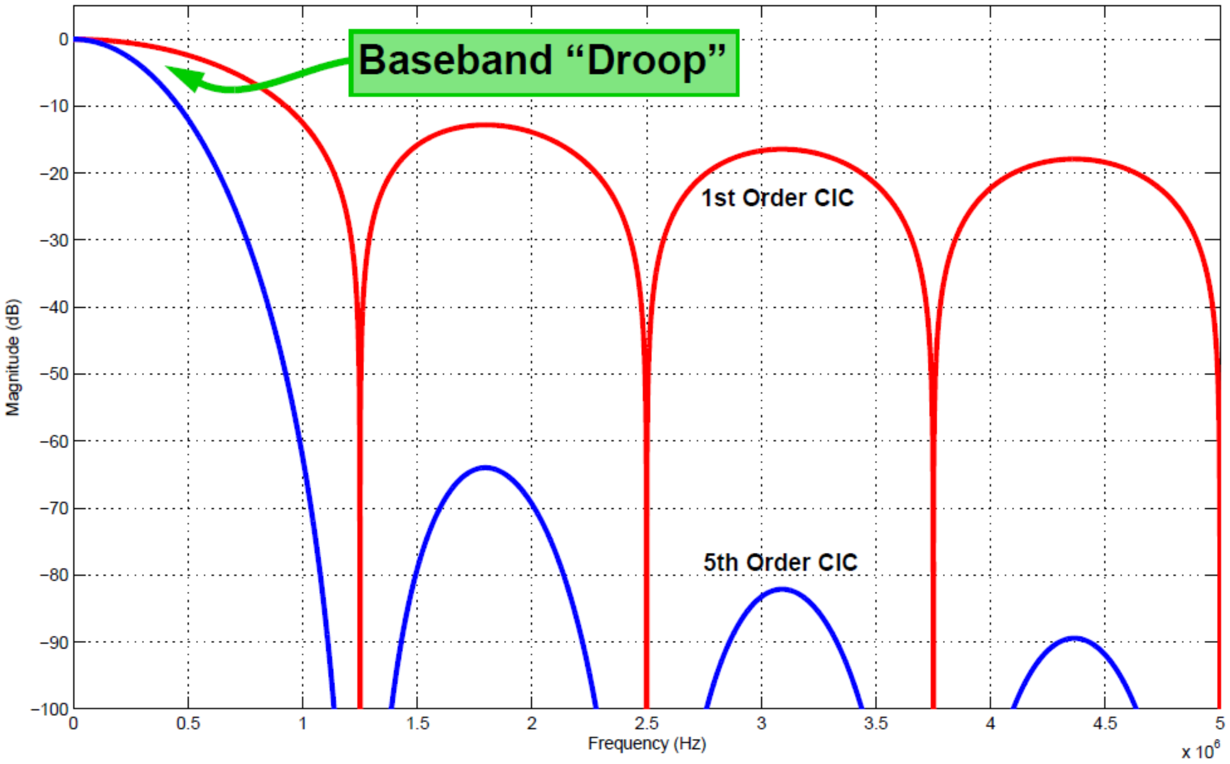
$$\frac{1-z^{-8}}{1-z^{-1}}\frac{1}{8} = (1+z^{-1}+z^{-2}+z^{-3}+z^{-4}+z^{-5}+z^{-6}+z^{-7})\frac{1}{8}$$

- **An M weight IC = M-1 Moving Average Filter**

CASCADE IC FILTER CIC

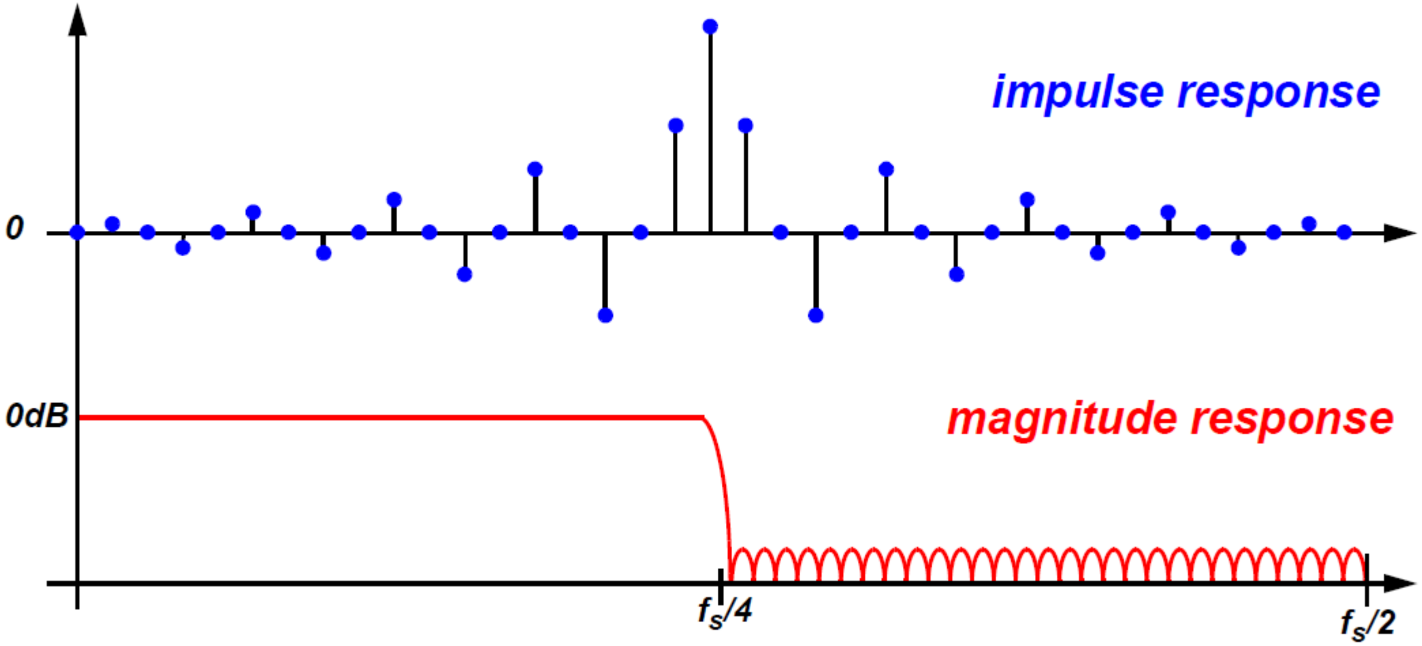
- Cascading IC producer better low pass characteristics.

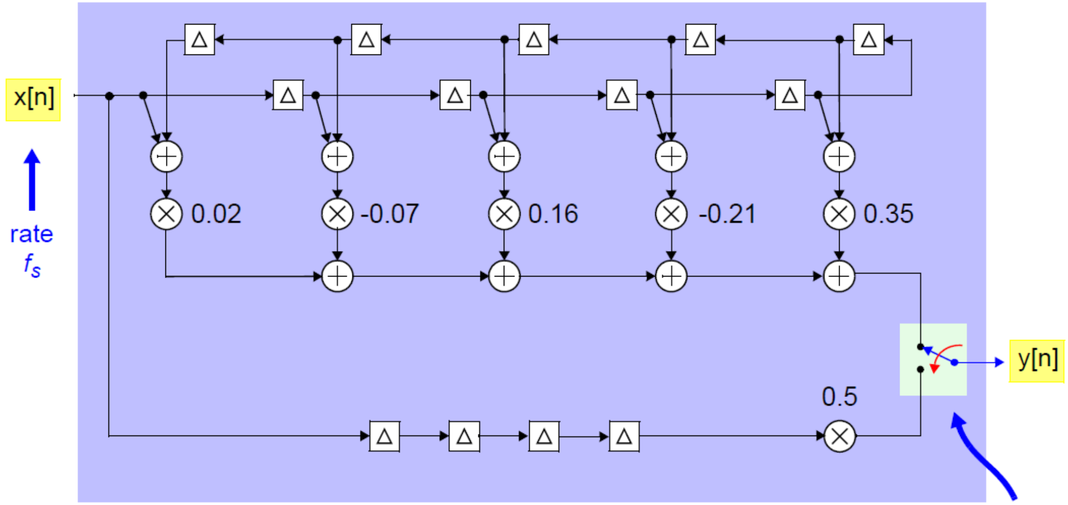




HALF BAND FILTER

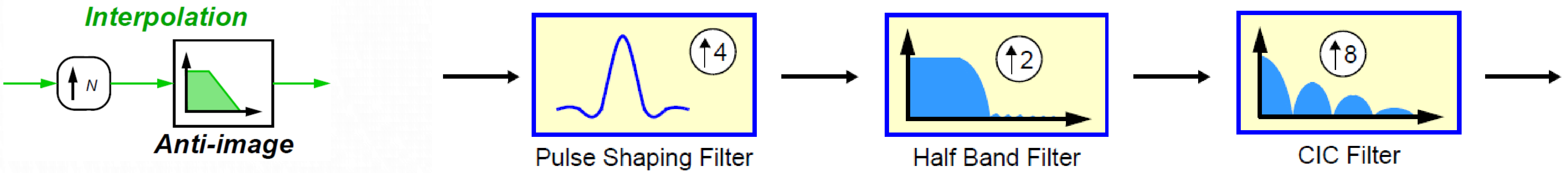
- Decimate by 2, very efficient implementation.

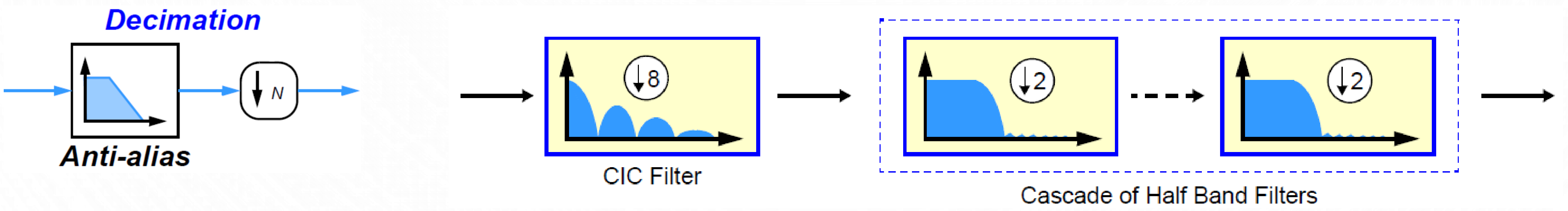




CIC FOR MULTIRATE FILTERING

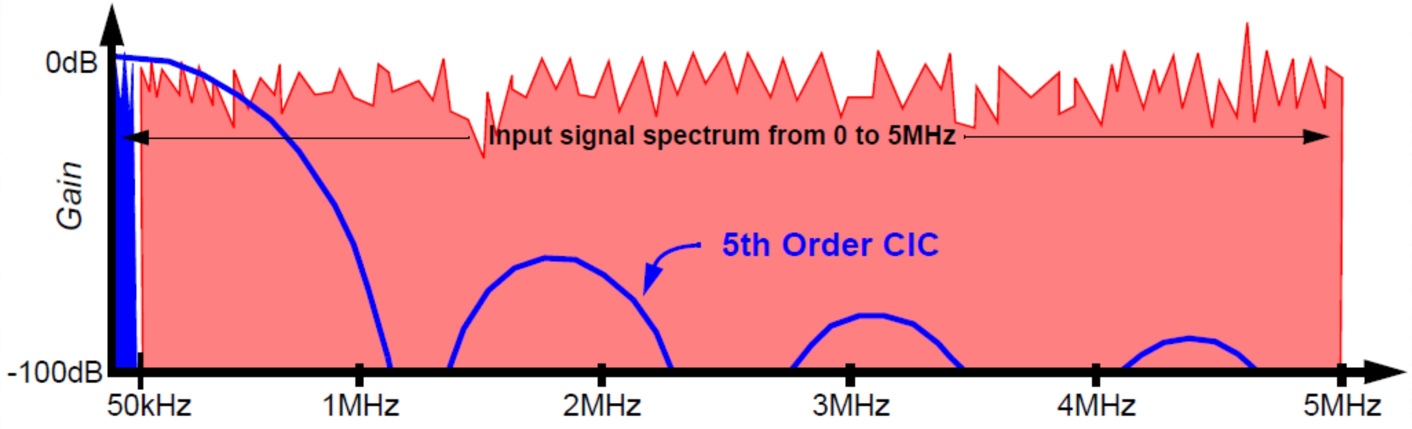
- CIC Filters have a sub-optimal frequency response but they are hardware cheap.
- First staged Decimation and final stage Interpolation with CICs and then use compensation FIR filters.

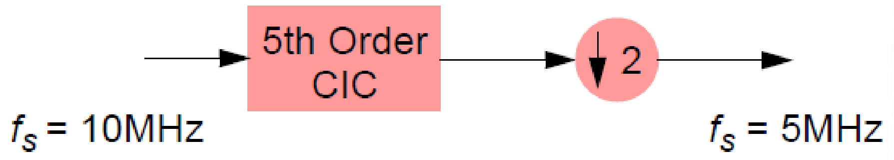




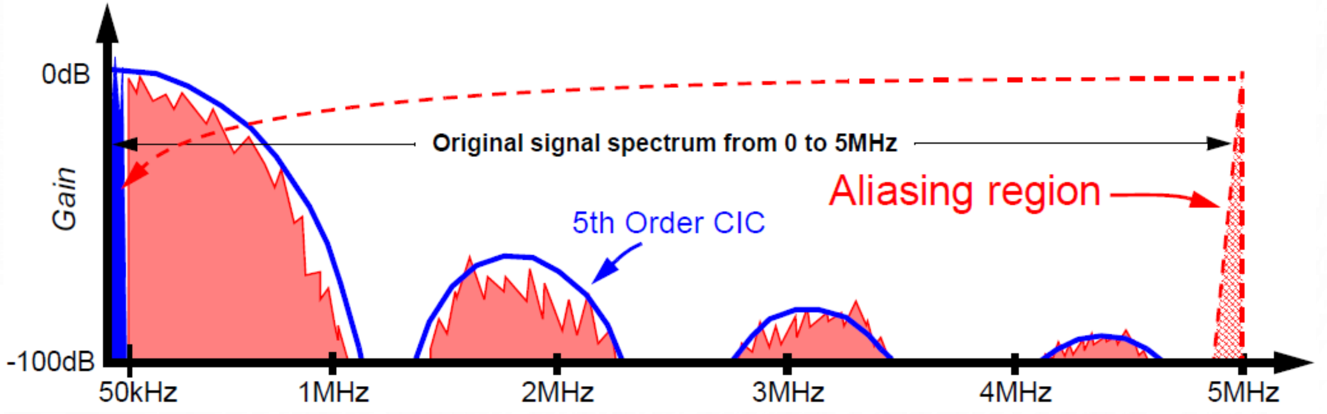
CIC DECIMATION

- Consider a 50Khz information signal we need to receive sampling at Fs=10Mhz.

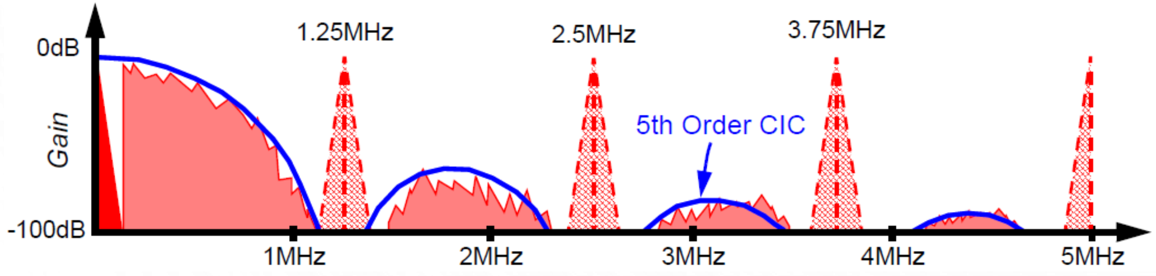




- Using 5 order CIC and down sampling by 2:

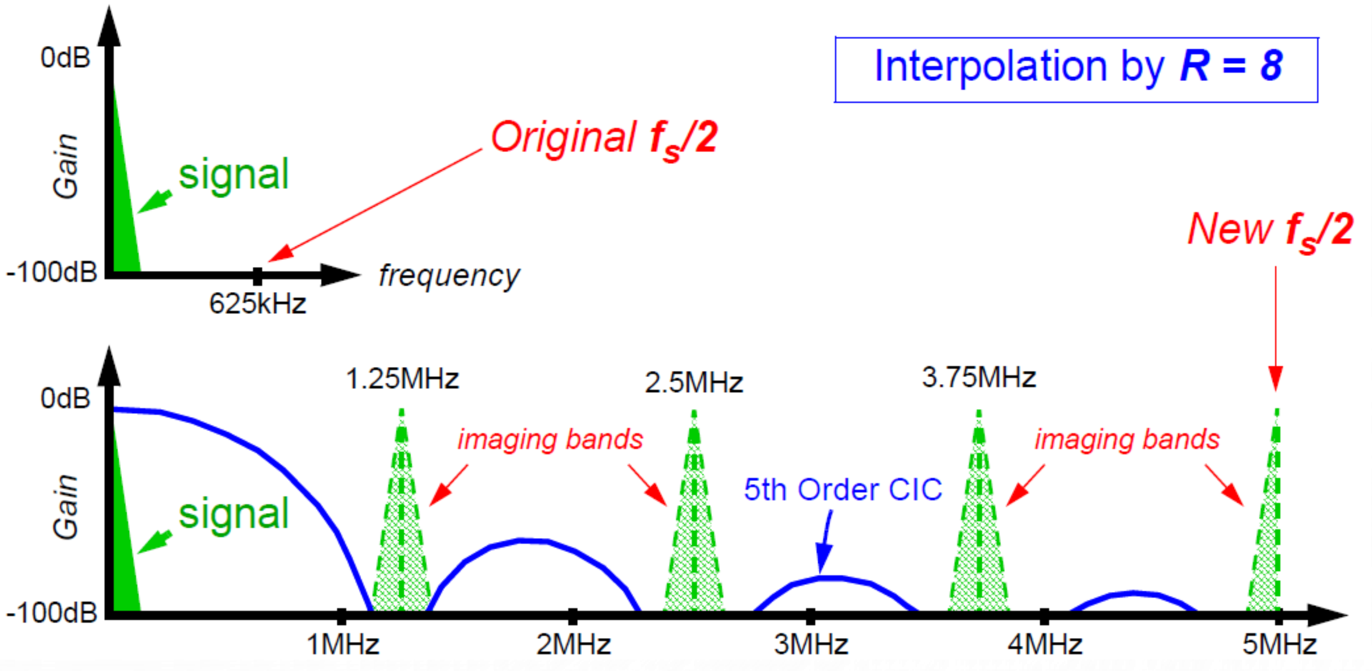


- Down sample by 8

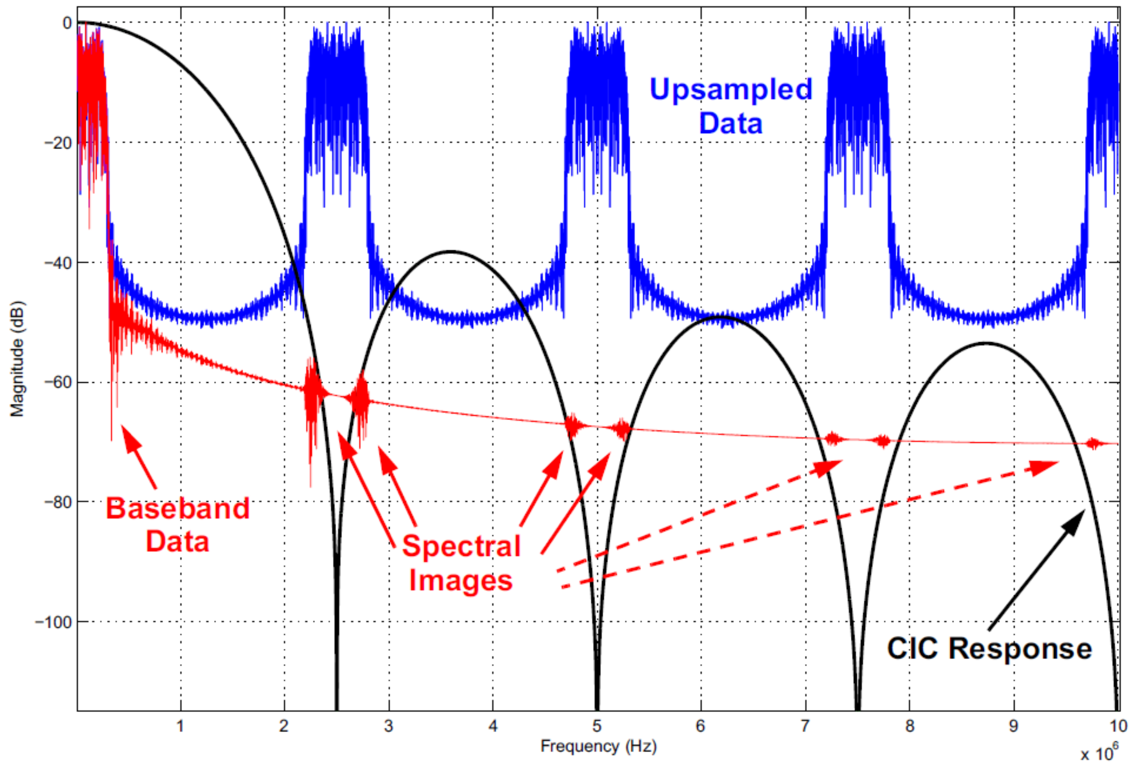


CIC FOR INTERPOLATION

- Similar happen when used for up-sampling



- DAC signal input



COMPENSATION FILTERING

- The droop on CIC filters is compensated using additional filters.
- Usually inverse SINC response FIR filters are used to compensate.