USC Viterbi

School of Engineering

*Center for Cyber-Physical Systems and the Internet of Things*

CCI

# SOFTWARE DEFINED RADIO

## USR SDR WORKSHOP, SEPTEMBER 2017
## PROF. MARCELO SEGURA

SESSION 3: PHASE AND FREQUENCY SYNCHRONIZATION

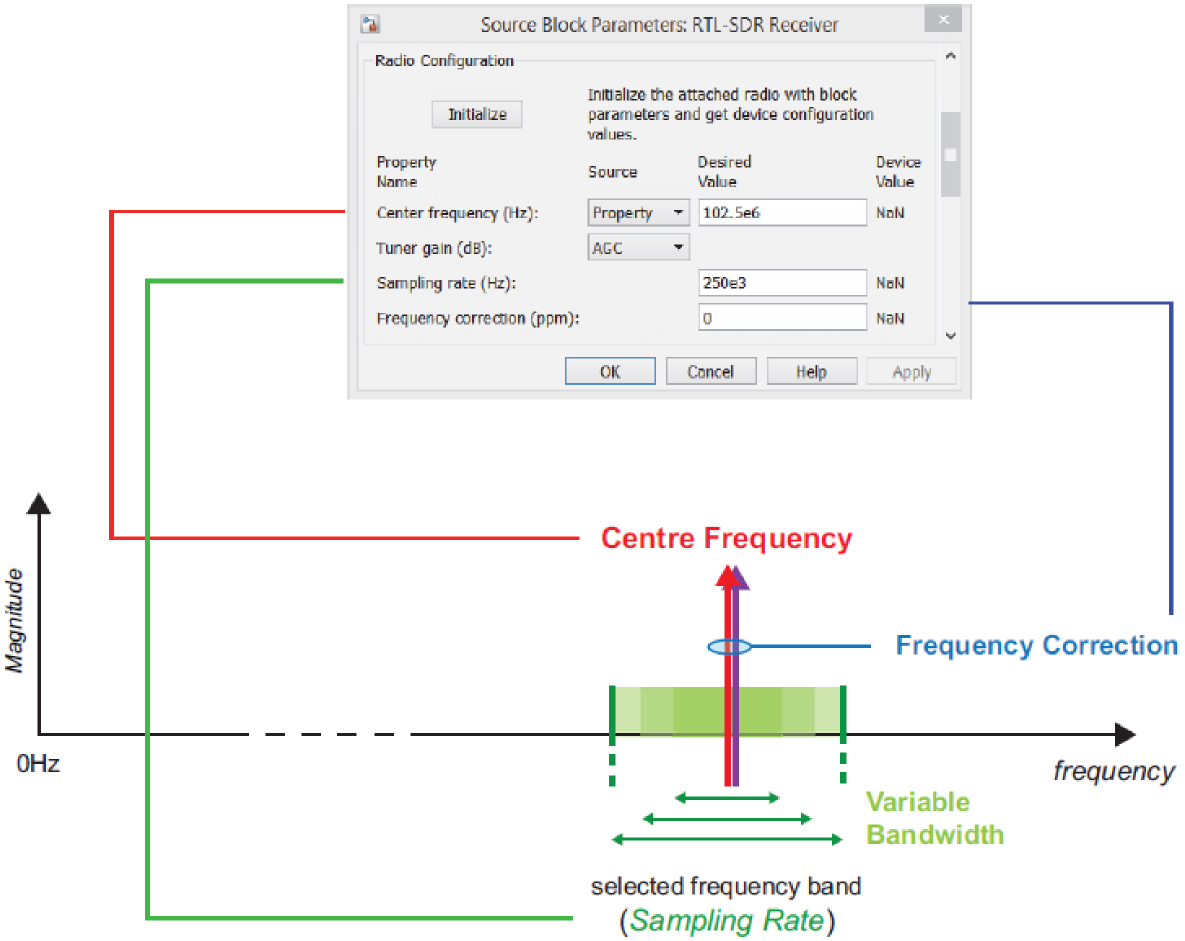
# TUNNING

- Tuning, consist on selecting the right value for the LO and the appropriated sampling rate.
- All the tuning parameters are setup on Simulink block.
- You should be carful with the LO difference

between SDR boards.

- On B200, the sample rate is defined by the

relation between clock and up/down sampling.



Source Block Parameters: RTL-SDR Receiver

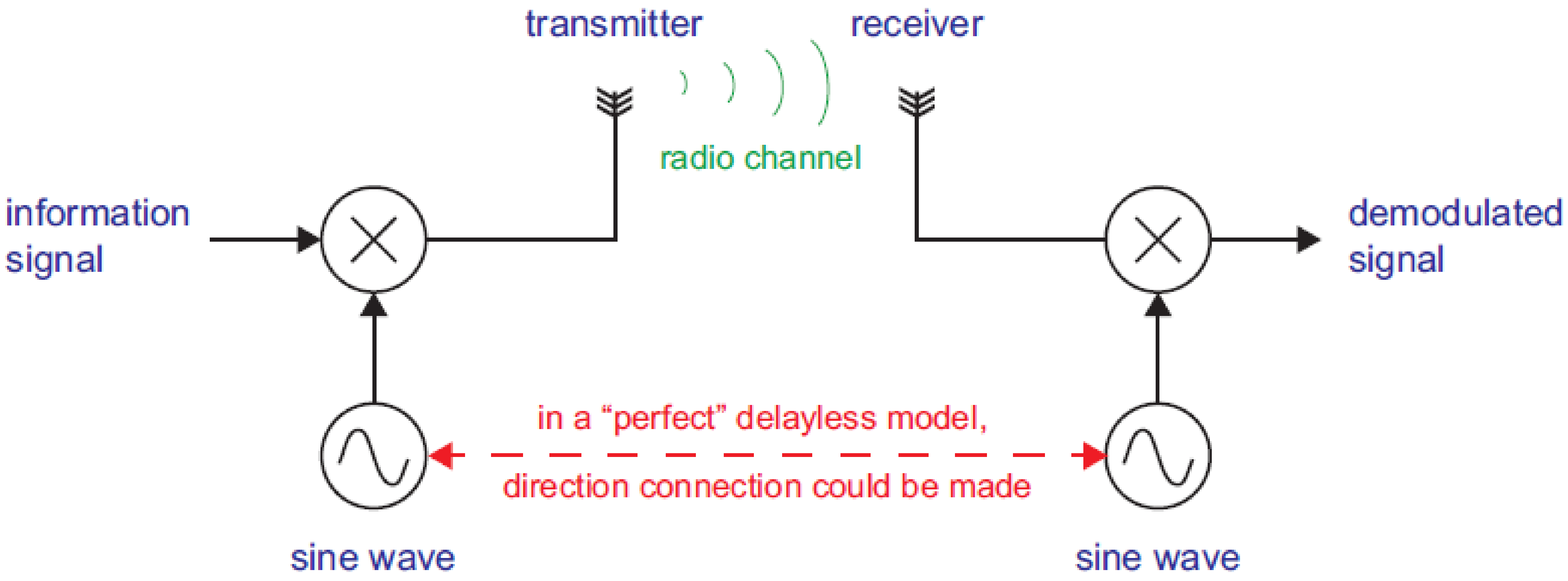
Radio Configuration

Initialize the attached radio with block parameters and get device configuration values.

| Property Name | Source | Desired Value | Device Value |
|---|---|---|---|
| Center frequency (Hz): | Property | 102.5e6 | NaN |
| Tuner gain (dB): | AGC | | |
| Sampling rate (Hz): | | 250e3 | NaN |
| Frequency correction (ppm): | | 0 | NaN |

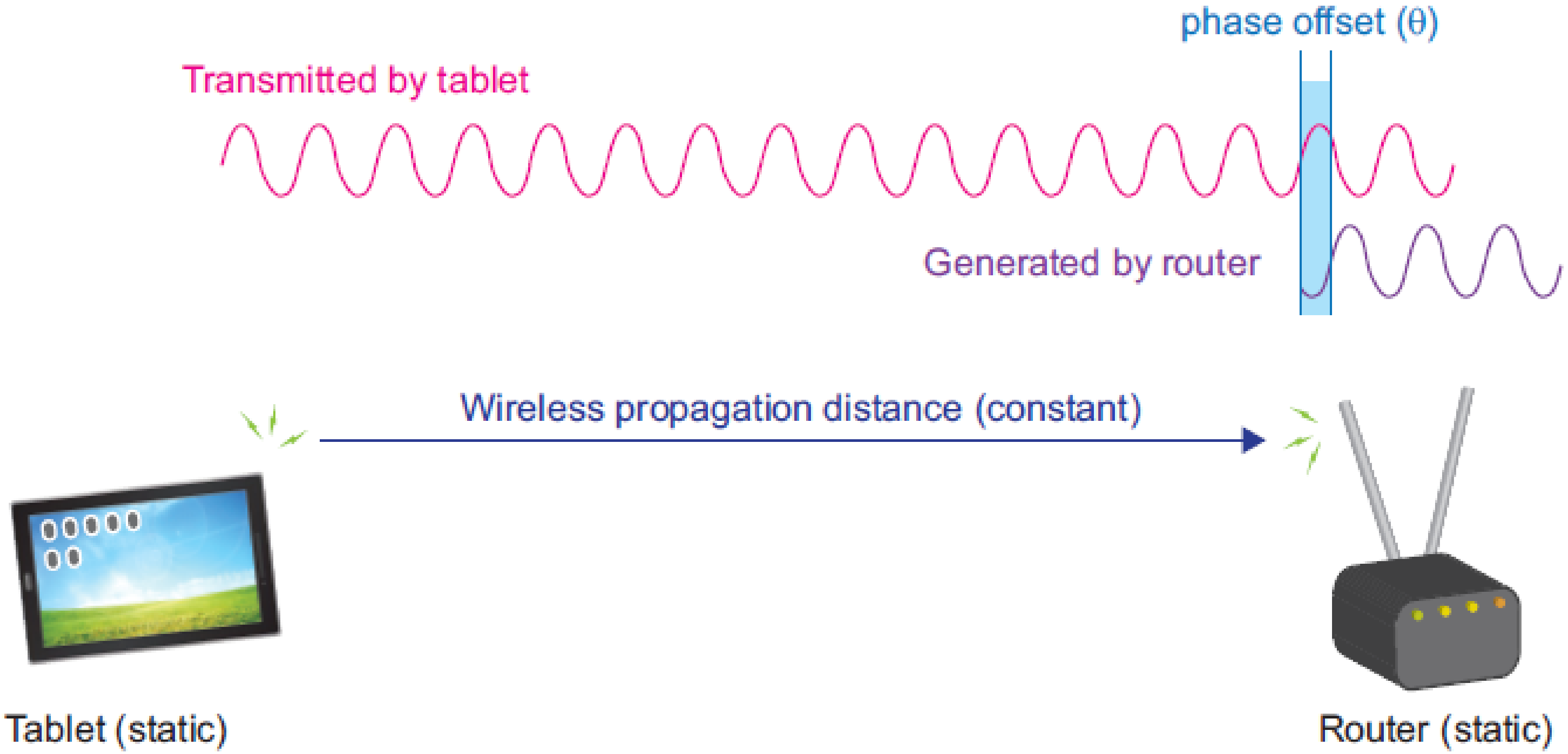
# THE SYNC PROBLEM

- Channel effects: A) Propagation delay B) frequency shift
- If we could consider No delay, always we have difference between LOs.



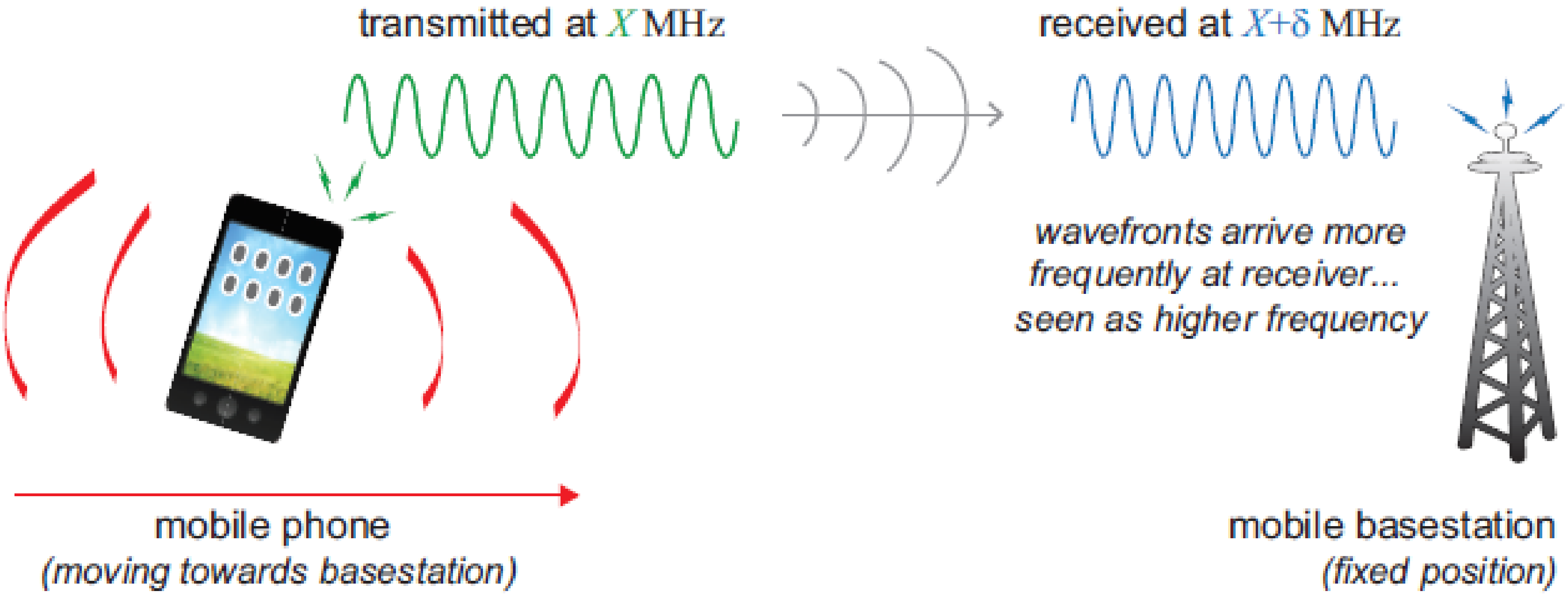
# PROPAGATION DELAY

- If TX ad RX are fixed position, we always have fixed phase offset.



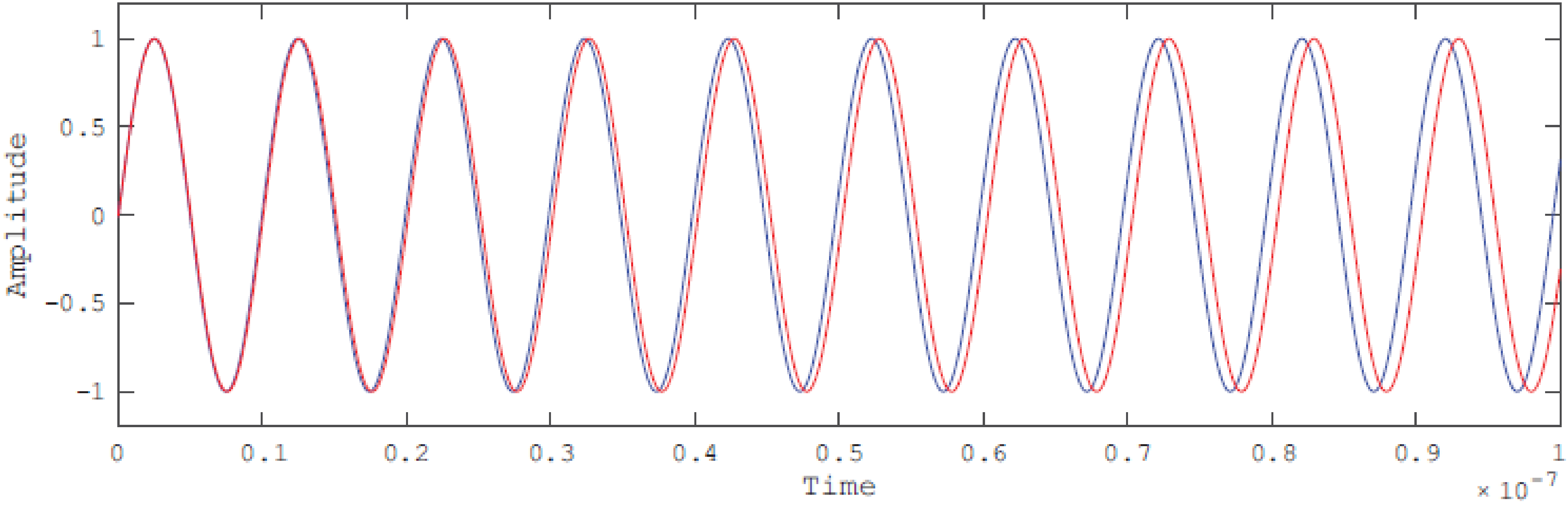
# FREQUENCY SHIFT

- If TX and RX moves, there will be a time variance phase shift that is equivalent to a frequency shift.
- Doppler effect.


transmitted at $X$ MHz
received at $X+\delta$ MHz
wavefronts arrive more frequently at receiver... seen as higher frequency
mobile phone (moving towards basestation)
mobile basestation (fixed position)

# HARDWARE EFFECTS

- LO change over time due to: temperature, manufacture process, ageing and others.
- Example: error of 5000ppm, f1=100,5Mhz, f2=99,5Mhz, Fc=100Mhz



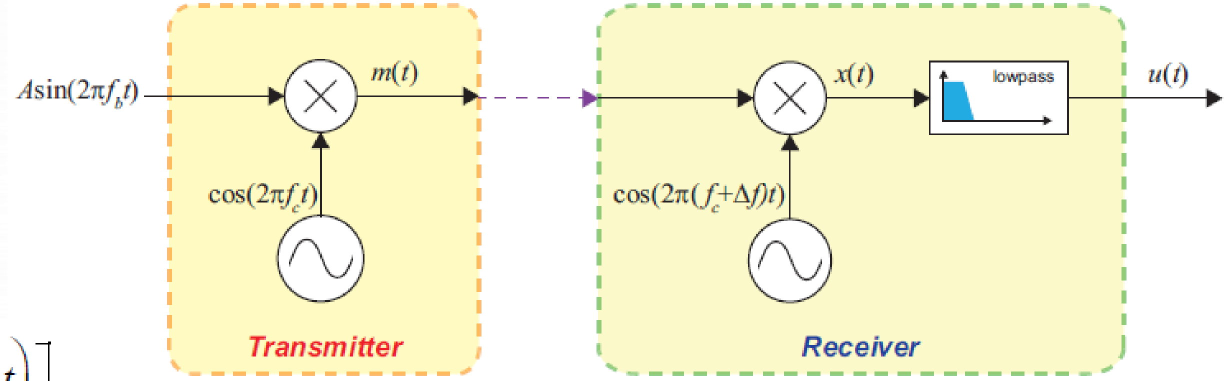
# COHERENT DEMODULATOR

- Demodulate with an LO that is not exactly the same….problems, so **Solutions:**
- Option 1: TX the carrier like DSB-TC (pros/con)
- Option 2: **Recovering the carrier from the modulated signal.**
- Modulated Signal (DSB-SC)

$$m(t) = \frac{A}{2}\left[\sin(2\pi(f_c+f_b)t) - \sin(2\pi(f_c-f_b)t)\right]$$

- Demodulated Signal

$$x(t) = \cos(2\pi(f_c+f_\Delta)t) \times \frac{A}{2}\left[\sin(2\pi(f_c+f_b)t) - \sin\left(2\pi(f_c-f_b)t\right)\right]$$



*lowpass filtered term*

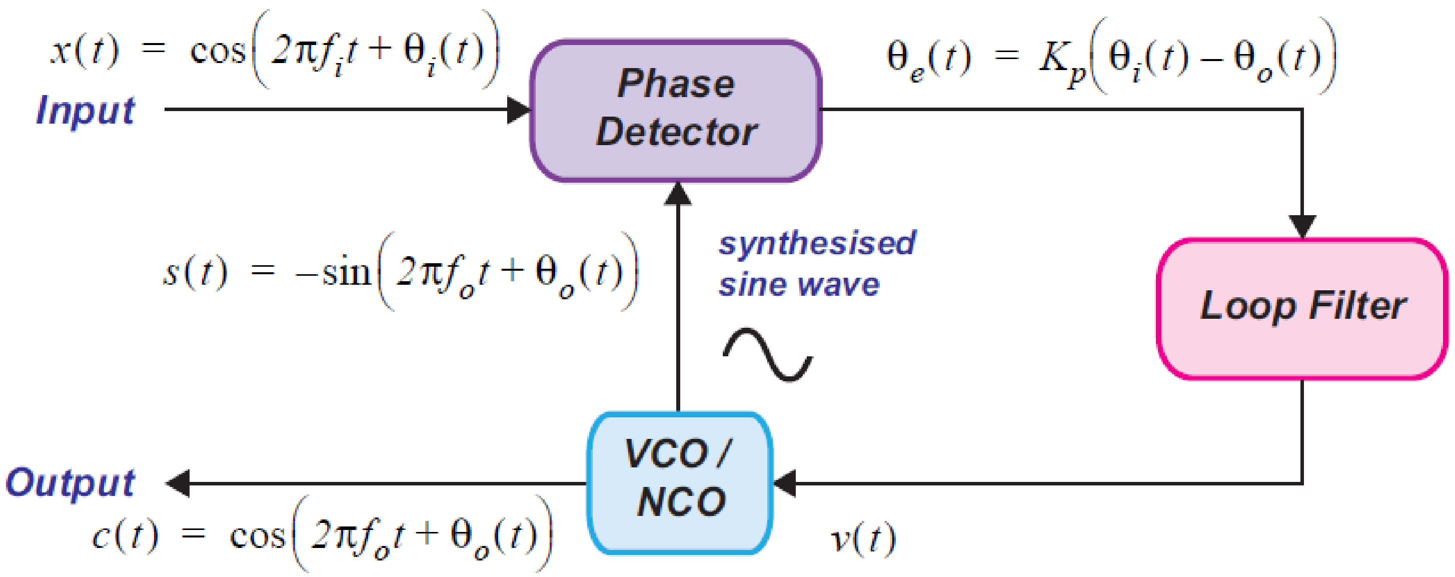
$$u(t) = \cancel{\frac{A}{4}\sin\left(2\pi(2f_c+f_\Delta+f_b)t\right)} - \frac{A}{4}\sin\left(2\pi(f_\Delta-f_b)t\right)$$
$$\cancel{-\frac{A}{4}\sin\left(2\pi(2f_c+f_\Delta-f_b)t\right)} + \frac{A}{4}\sin\left(2\pi(f_\Delta+f_b)t\right)$$

*lowpass filtered term*

$$u(t) = \frac{A}{4}\left[\sin(2\pi(f_b+f_\Delta)t) + \sin(2\pi(f_b-f_\Delta)t)\right]$$

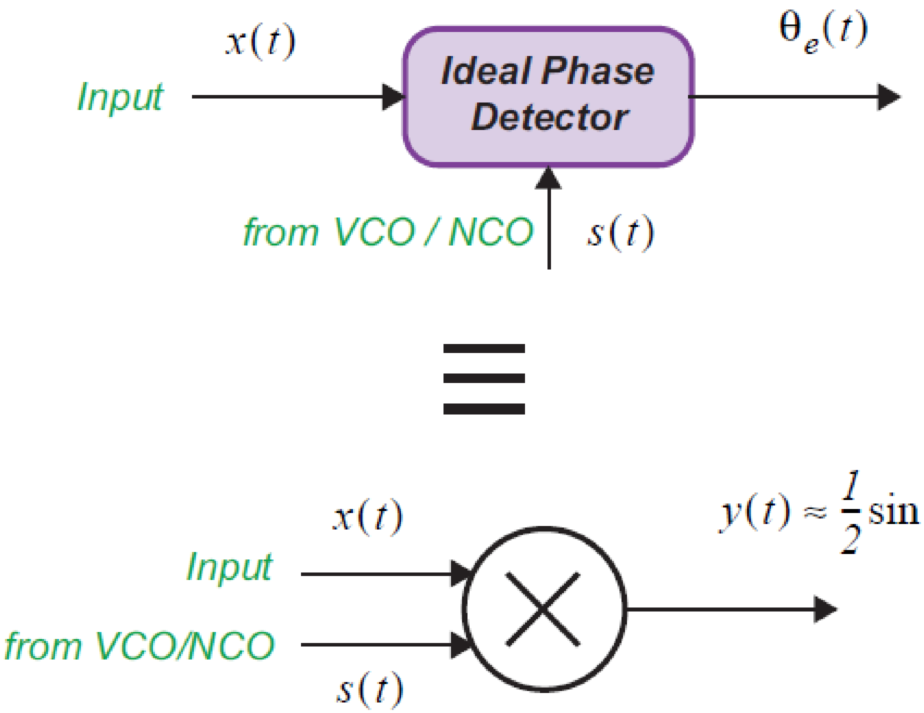
# PHASE LOCK LOOP, REVIEW

- The PLL is the fundamental component on every coherent receiver.
- PLL:
  - Phase Detector: the output is proportional to the phase difference between received signal and locally generated.
  - Controlled Oscillator: it is a VCO for analog receiver and NCO for digital receiver.
  - Loop filter: Filter acts upon the output of the Phase Detector to remove unwanted high frequency terms, and produce the signal that drives the VCO or NCO.


$x(t) = \cos\left(2\pi f_i t + \theta_i(t)\right)$
Input
Phase Detector
$\theta_e(t) = K_p\left(\theta_i(t) - \theta_o(t)\right)$
$s(t) = -\sin\left(2\pi f_o t + \theta_o(t)\right)$
synthesised sine wave
Loop Filter
Output
VCO / NCO
$c(t) = \cos\left(2\pi f_o t + \theta_o(t)\right)$
$v(t)$

# PHASE DETECTOR

- The phase error is proportional to the phase difference: $$\theta_e(t) = K_p\left(\theta_i(t) - \theta_o(t)\right)$$
- Implemented as a multiplier.
- If the difference is small, the mixing approach to the difference.



$$y(t) \approx \tfrac{1}{2}\sin\left(\theta_i(t) - \theta_o(t)\right) + \textit{high frequency terms}$$

$$y(t) = x(t) \times s(t)$$

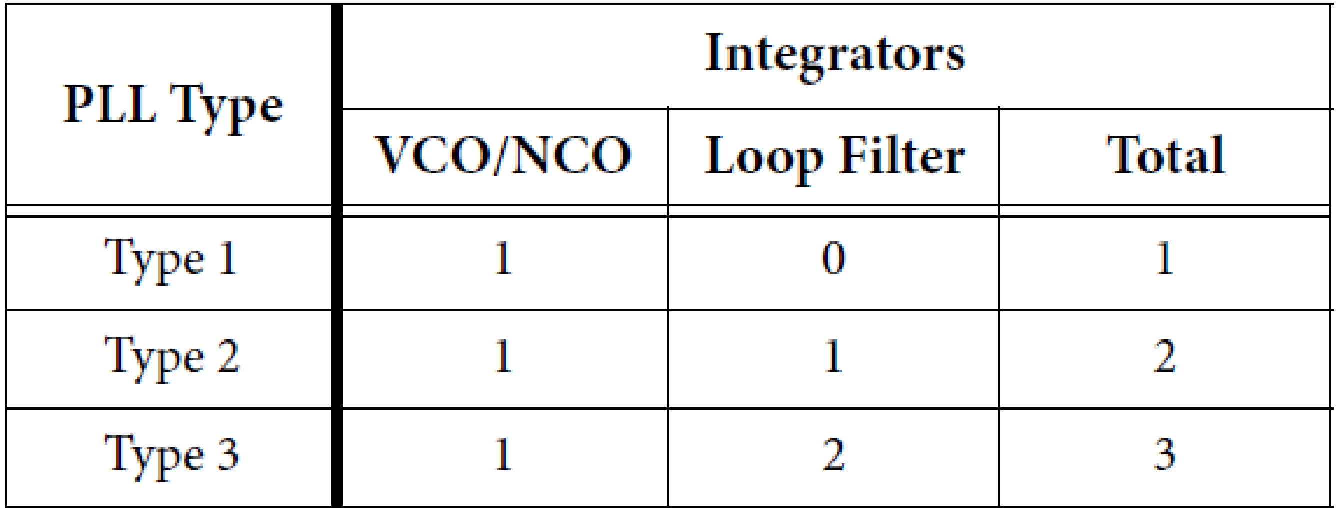
$$= \cos\left(2\pi f_i t + \theta_i(t)\right) \times -\sin\left(2\pi f_o t + \theta_o(t)\right)$$

$$y(t) = \underbrace{\tfrac{1}{2}\sin\left(\theta_i(t) - \theta_o(t)\right)}_{\text{low frequency term}} \underbrace{-\,\tfrac{1}{2}\sin\cancel{\left(4\pi f_i(t) + \theta_i(t) + \theta_o(t)\right)}}_{\text{high frequency term}}$$

$$y(t) \approx \tfrac{1}{2}\left(\theta_i(t) - \theta_o(t)\right)$$

# LOOP FILTER

- The design of the loop filter is vital in defining the overall characteristics and behavior of the PLL.
- The PLL type corresponds to the number of integrators in the loop, including the one that add the VCO/NCO.



| PLL Type | Integrators | | |
|---|---|---|---|
| | VCO/NCO | Loop Filter | Total |
| Type 1 | 1 | 0 | 1 |
| Type 2 | 1 | 1 | 2 |
| Type 3 | 1 | 2 | 3 |

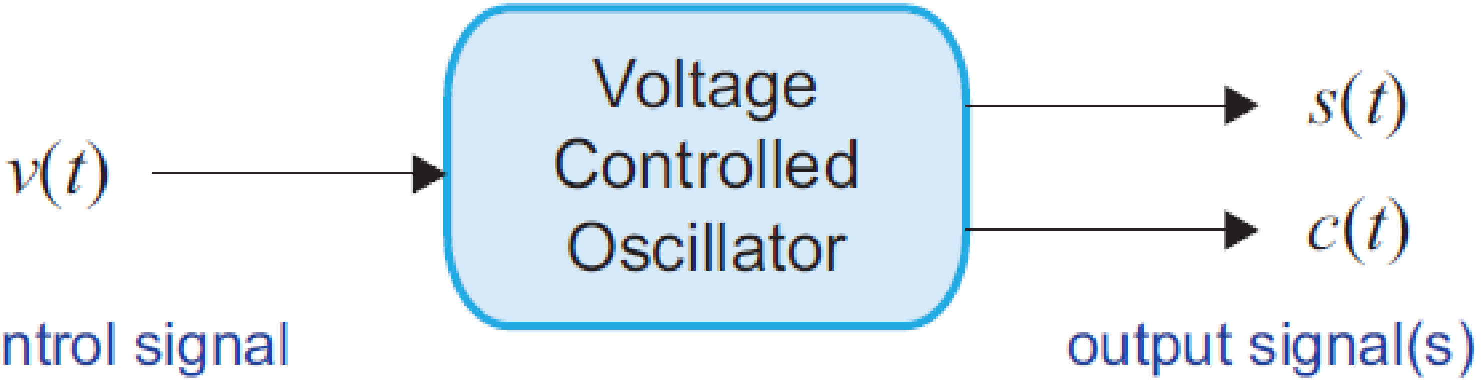
# CONTROLLED OSCILLATOR

- The VCO control signal is the filtered phase difference v(t)
- The estimated phase at instant “t” is :

$$\hat{\theta}(t) = k_o \int_0^t v(t)\, dt$$

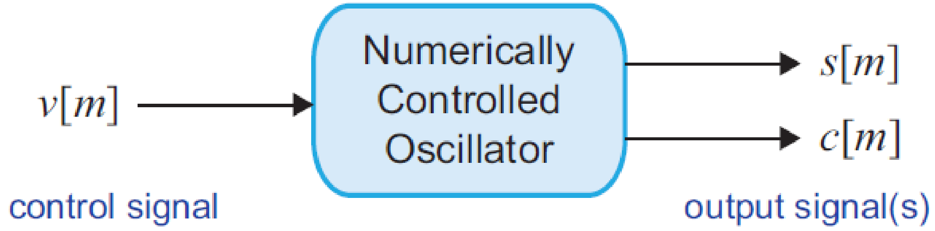
- *k0* is the sensibility of VCO

$$c(t) = \cos\left(2\pi f_o t + \hat{\theta}(t)\right)$$



# NCO: NUMERICALLY CONTROLLED OSCILLATORS

- The digital version of VCO.



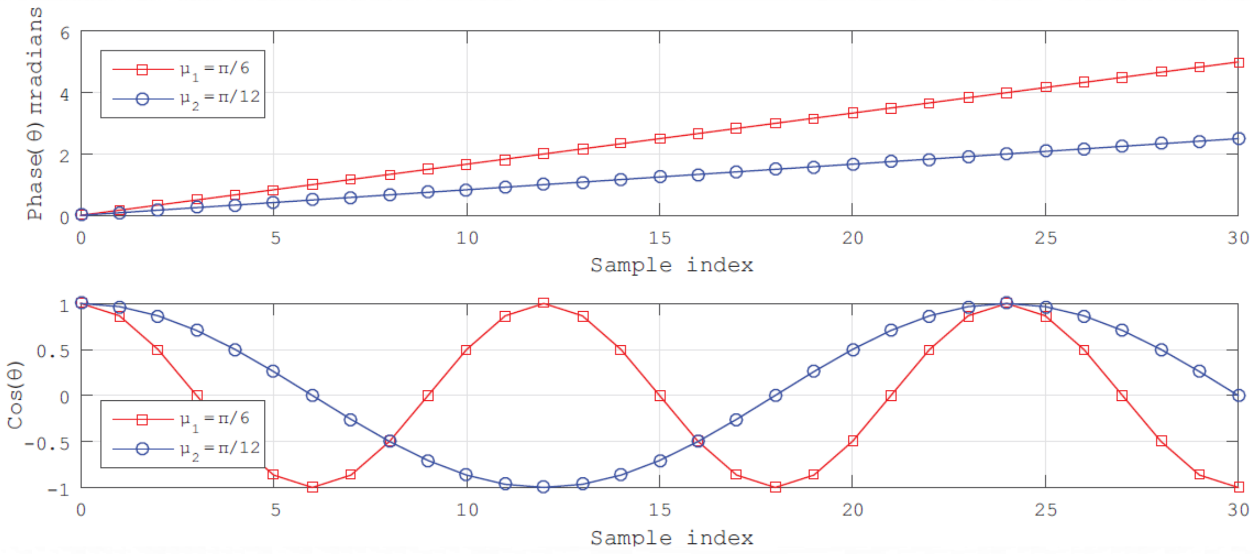
$$c[m] = \cos\left(2\pi f_o m T + \hat{\theta}[m]\right)$$

$$\hat{\theta}[m] = K_o \sum_{m=0}^{M} v[m]$$

$$\hat{\theta}[m] = \hat{\theta}[m-1] + \mu[m]$$

$$\mu = \frac{2\pi f_d}{f_s}$$

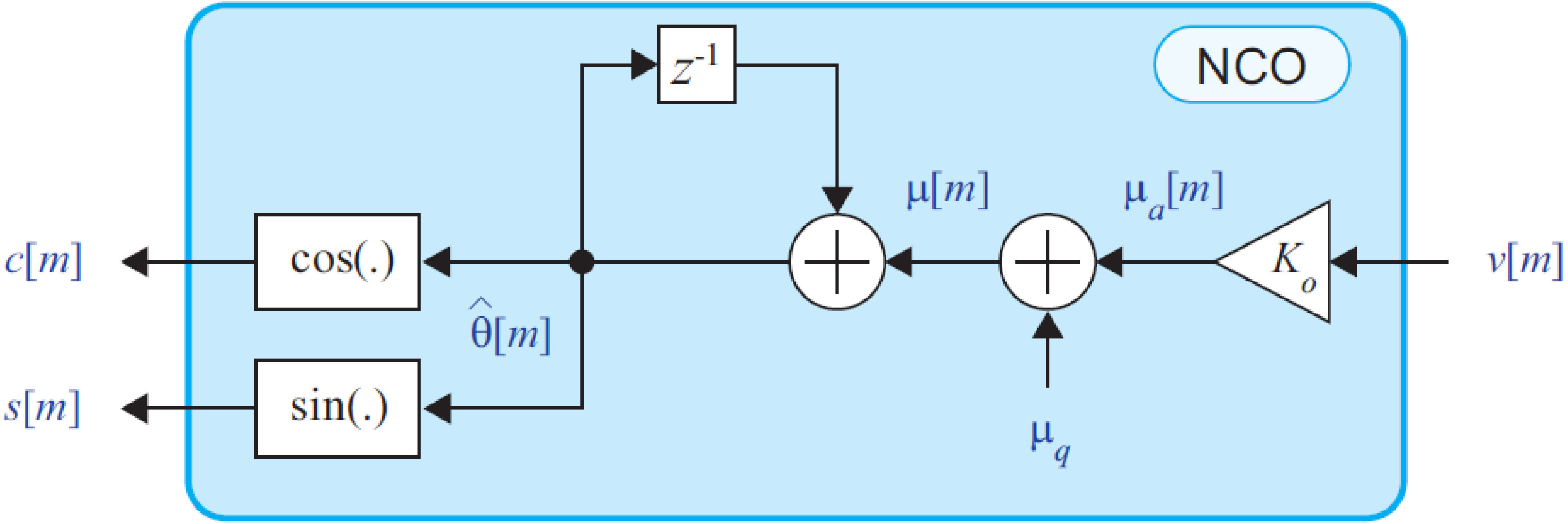
- Different frequencies are created from different step size.

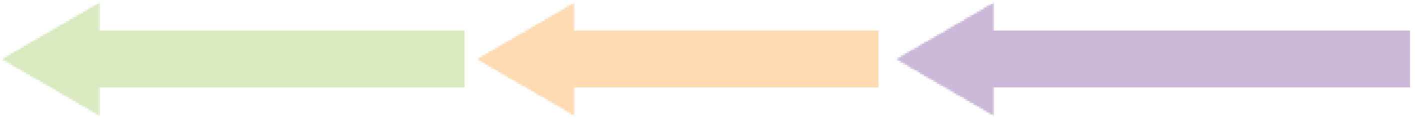


# NCO

- To follow a frequency change, an adjustment term is needed.

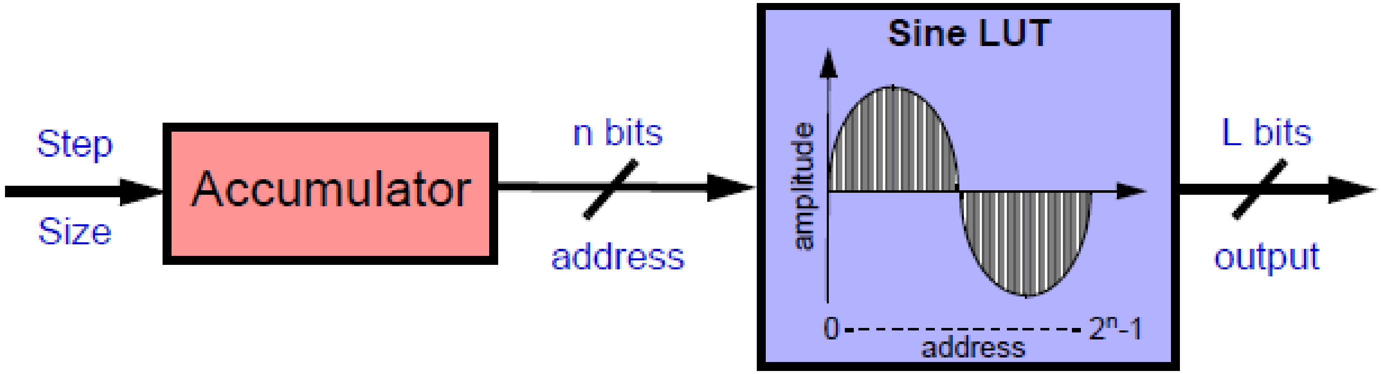
$\hat{\theta}[m] = \hat{\theta}[m-1] + \mu[m]$  $\mu[m] = \mu_q + \mu_a[m]$  $\mu_a[m] = K_o v[m]$





# NCO: IMPLEMENTATION ON FPGA

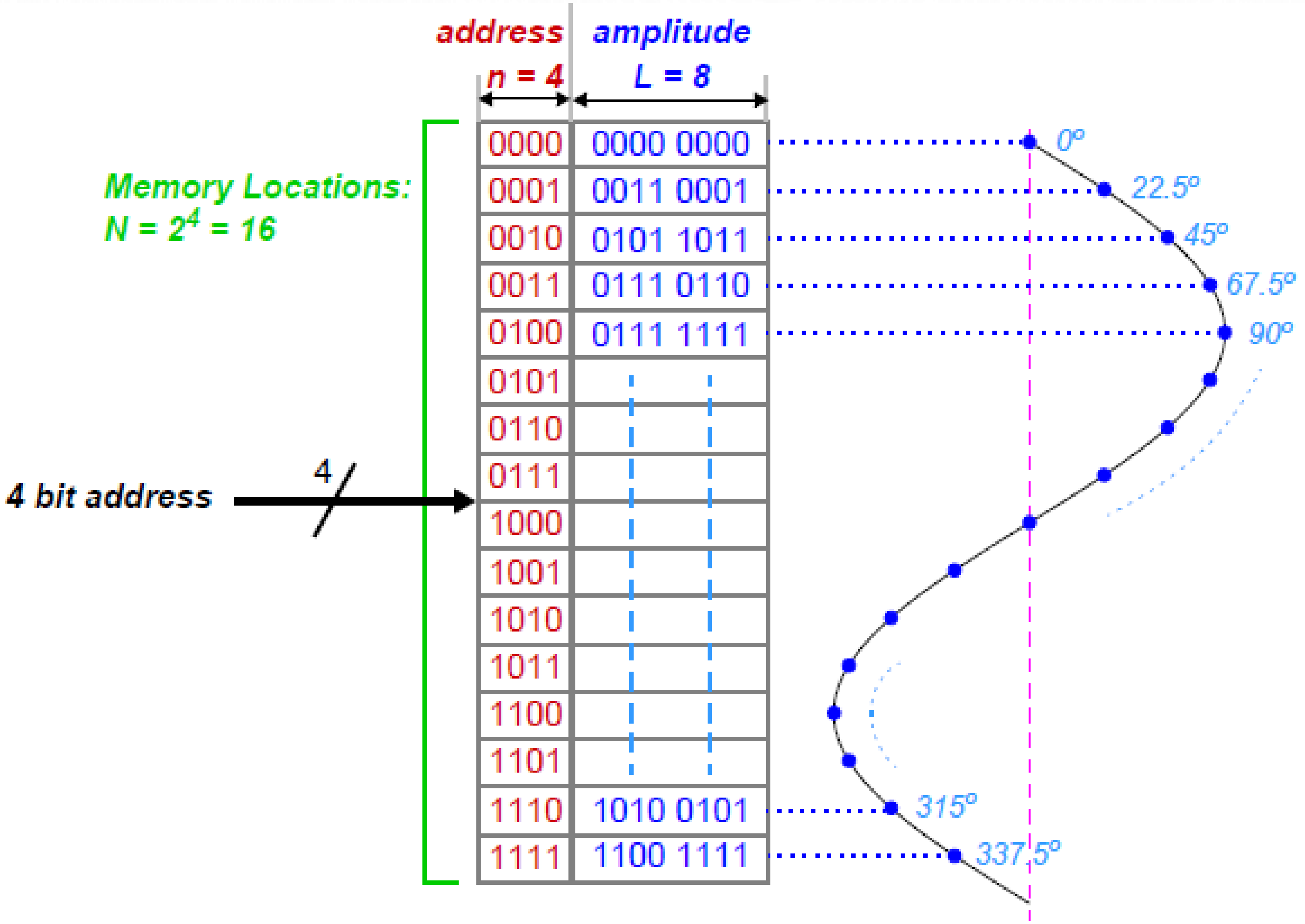
- The simplest operation inside FPGA could be up/down conversion to intermediate frequency.
- NCO are usually implemented on LUTs. Also called Digital Direct Synthesizer (DDS).



- The LUT has $N=2^n$ size, where n is the numbers of bits that accumulator generate.
- The amplitude resolution of the signal depends on the number of **outputs bits L,** and the frequency resolution depends on LUT size, n.

# NCO ON FPGA

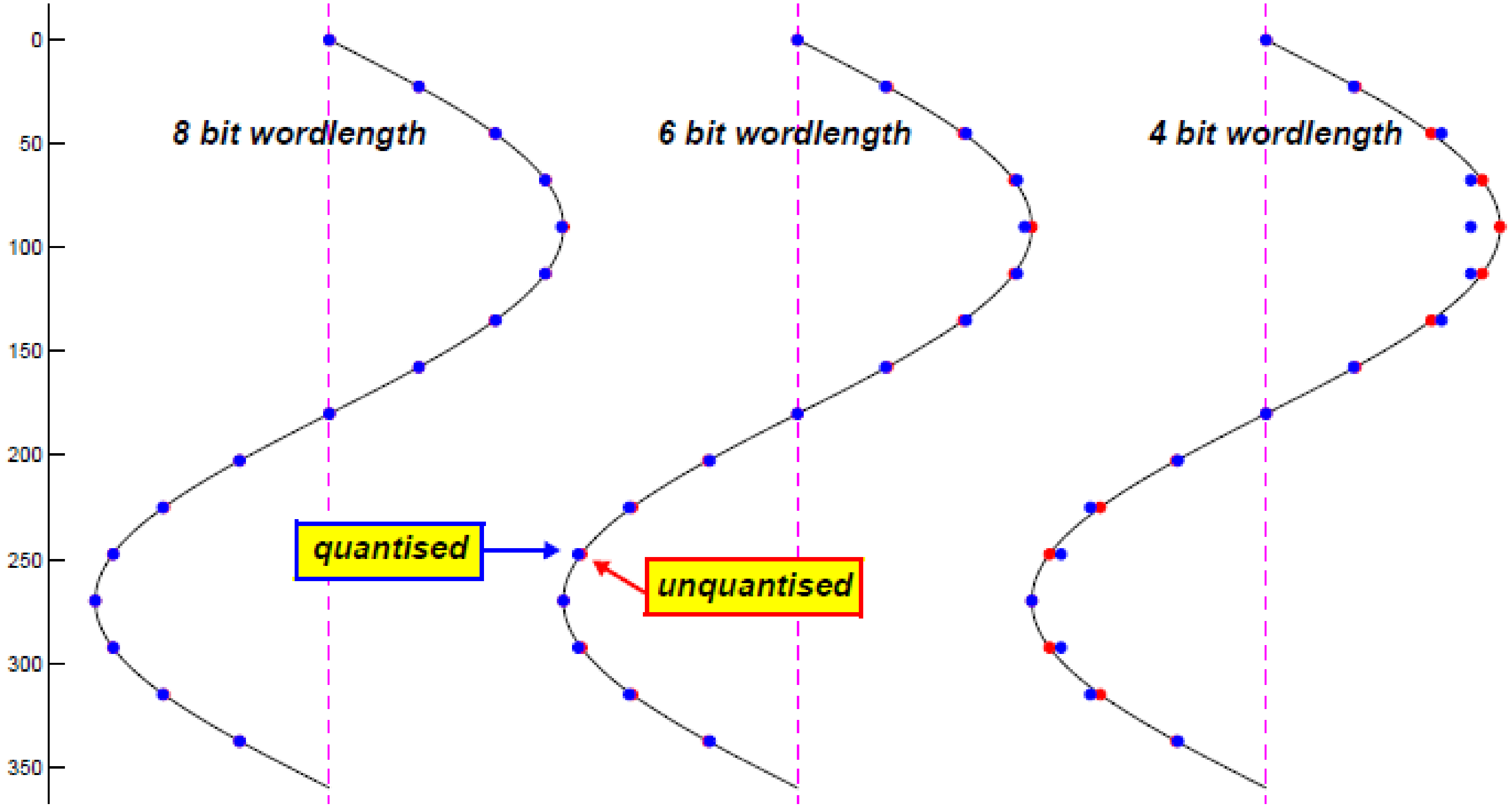
- Frequency and amplitude resolution



| address<br>n = 4 | amplitude<br>L = 8 |
|---|---|
| 0000 | 0000 0000 |
| 0001 | 0011 0001 |
| 0010 | 0101 1011 |
| 0011 | 0111 0110 |
| 0100 | 0111 1111 |
| 0101 | |
| 0110 | |
| 0111 | |
| 1000 | |
| 1001 | |
| 1010 | |
| 1011 | |
| 1100 | |
| 1101 | |
| 1110 | 1010 0101 |
| 1111 | 1100 1111 |

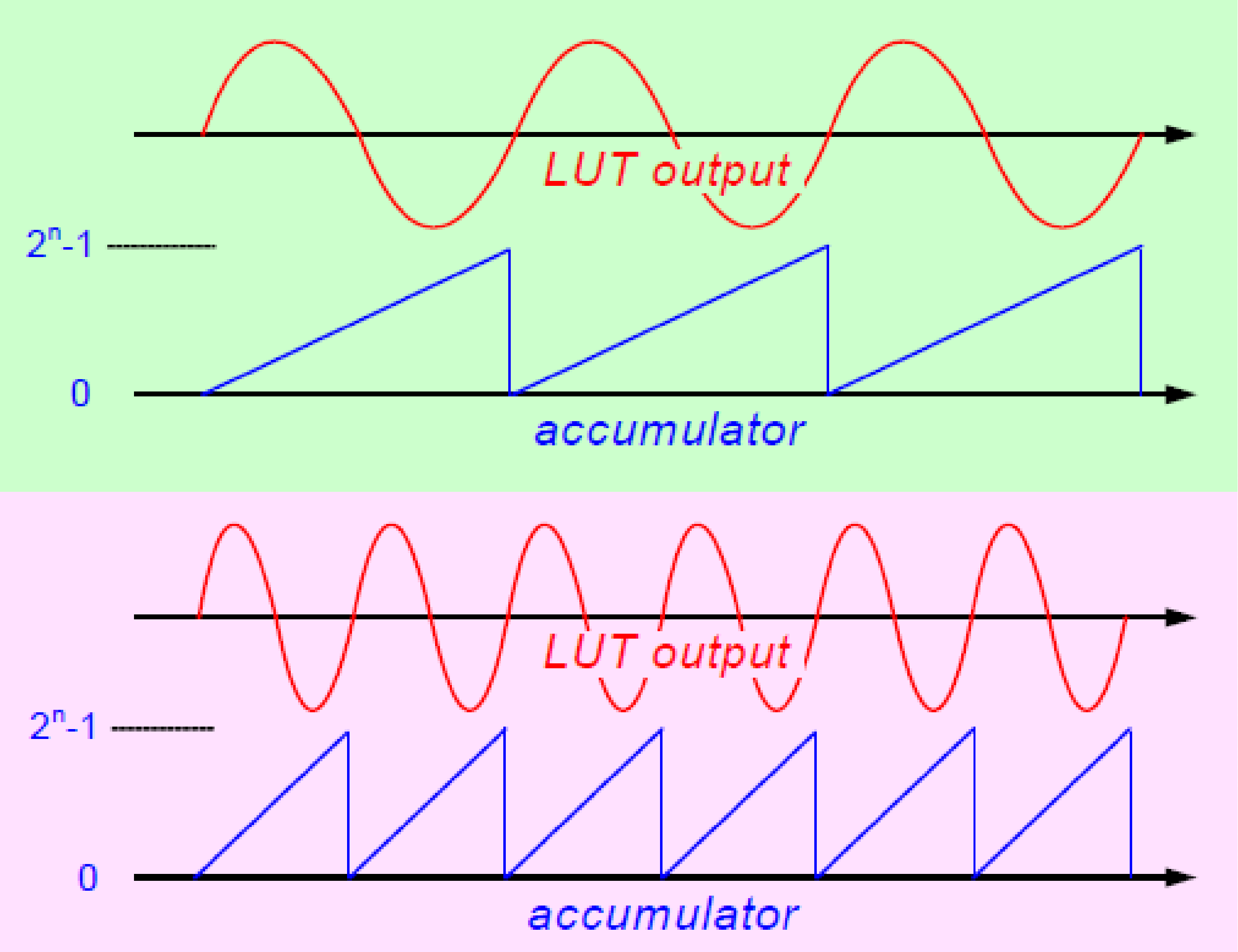
# NCO ON FPGA

- Quantization effect, L



# NCO ON FPGA

- Frequency control is done by the **step** of Accumulator



# NCO ON FPGA

- The Accumulator step is determined by:
  - N: number s entries on the LUT.
  - Fs: sampling frequency
  - Fd: desired frequency

$$\mu = N \frac{f_d}{f_s}$$

- Example 8 bits, N=256, fs=10Mhz, fd=2.5Mhz

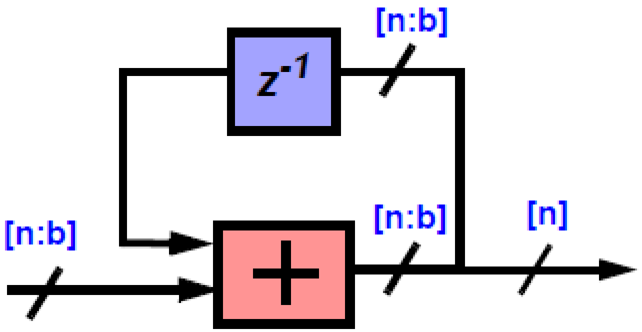
$$\mu = 256 \frac{2.5MHz}{10MHz} = 64$$

- If we need 2.4Mhz??

$$\mu = 256 \frac{2.4MHz}{10MHz} = 61.44 \ldots$$

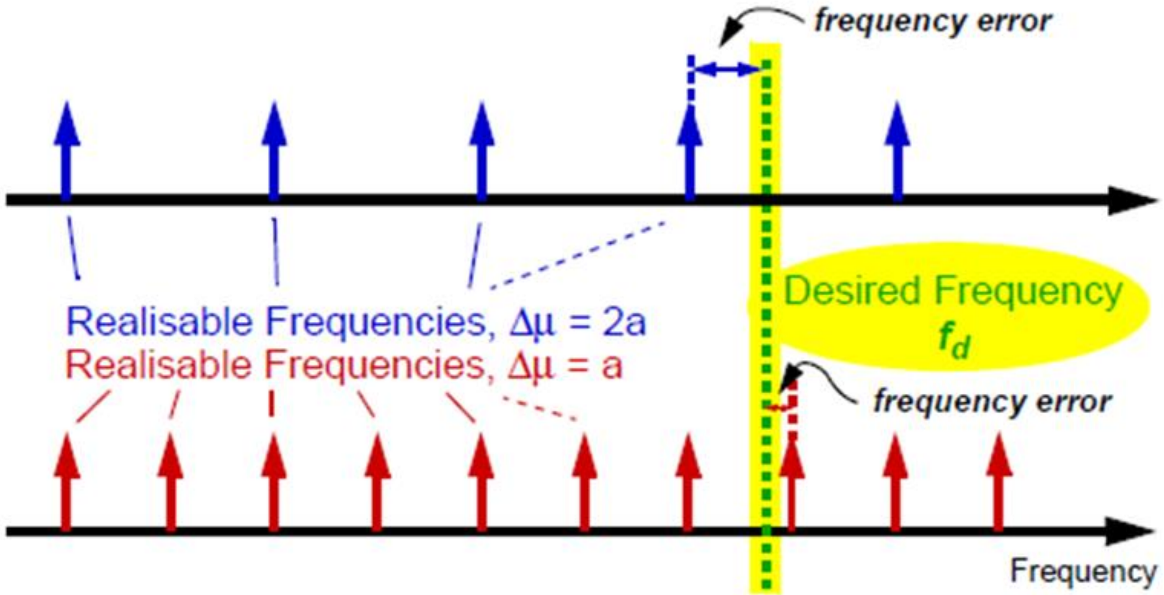
- We need to add a fractional part to the ACC.
- The step will have an integer and a fractional part [n:b]
- μ=61.4375 [8:4]

$$\mu \frac{f_s}{N} = 2,399,902Hz$$



# NCO ON FPGA

- Frequency resolution: depends on steps differences. $\Delta\mu = \frac{1}{2^b}$
- The fractional bits should be selected following the desired frequency resolution.


frequency error
Realisable Frequencies, Δμ = 2a
Realisable Frequencies, Δμ = a
Desired Frequency
$f_d$
frequency error
Frequency

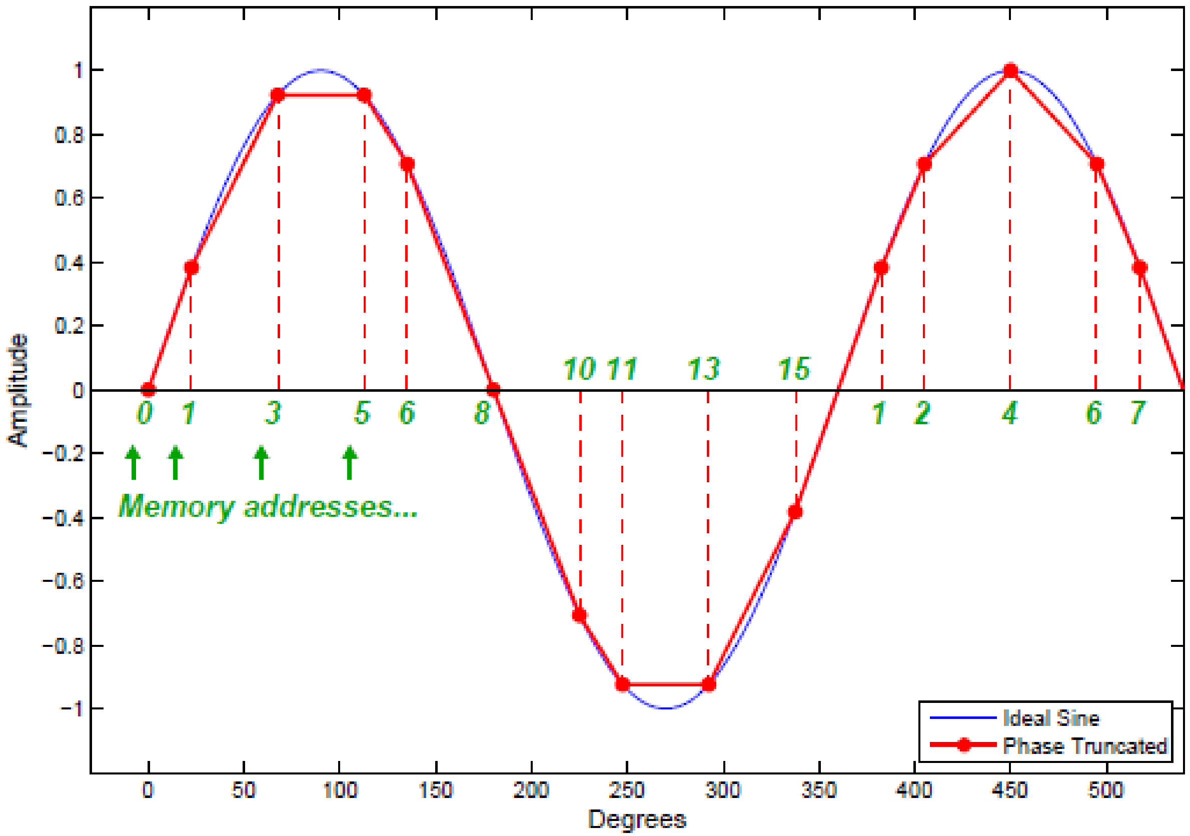
- Frequency resolution $\Delta$fa:

$$\Delta f_a = \Delta\mu \frac{f_s}{N} = \frac{f_s}{2^b N}$$

# NCO ON FPGA

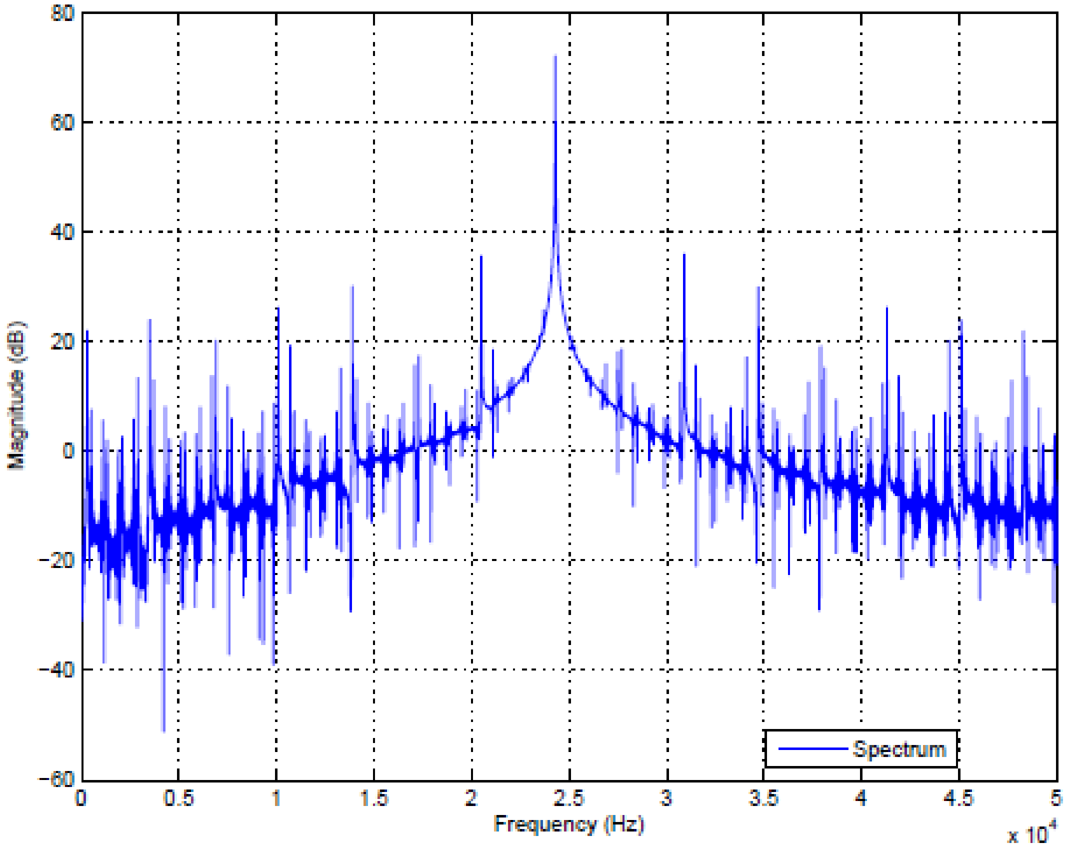
- Truncated error: if the step is μ=1.7, then spurious appear doe to truncate .

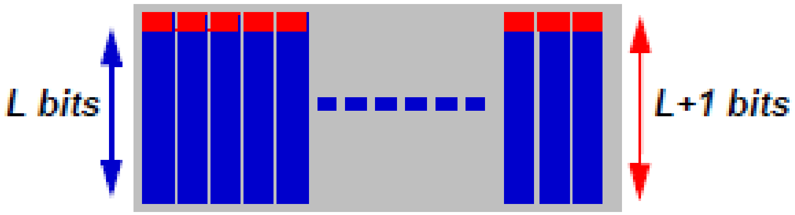
| Sample | Accum. | Address |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 1.7 | 1 |
| 2 | 3.4 | 3 |
| 3 | 5.1 | 5 |
| 4 | 6.8 | 6 |
| 5 | 8.5 | 8 |
| 6 | 10.2 | 10 |
| 7 | 11.9 | 11 |
| 8 | 13.6 | 13 |
| 9 | 15.3 | 15 |
| 10 | 1.0 | 1 |
| 11 | 2.7 | 2 |
| 12 | 4.4 | 4 |
| 13 | 6.1 | 6 |
| 14 | 7.8 | 7 |



# NCO ON FPGA

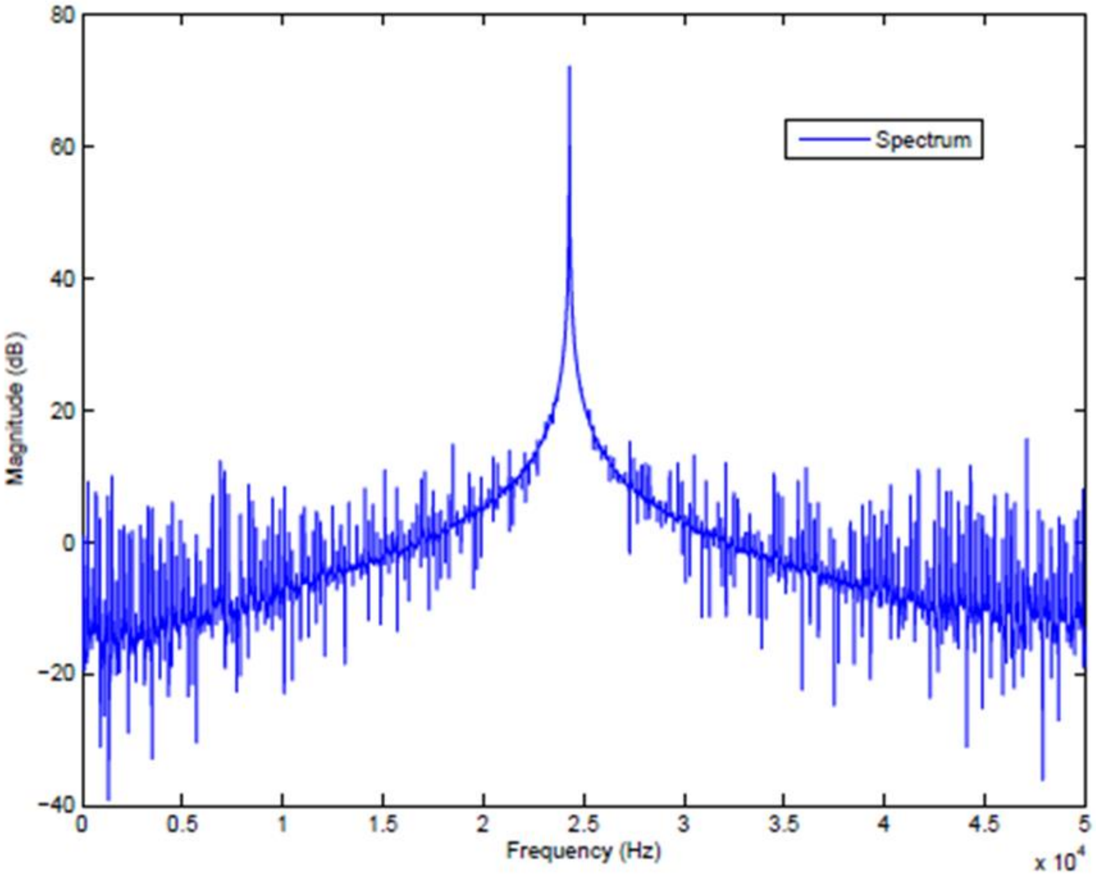
- TRUNCATED ERROR due to small N.
- Fs: 100kHz, fd: 24.3kHz, N:6, [n:b]=[**6**:16], **L=32**

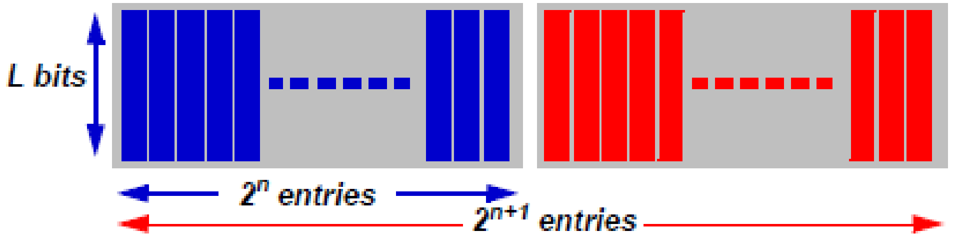




# NCO ON FPGA

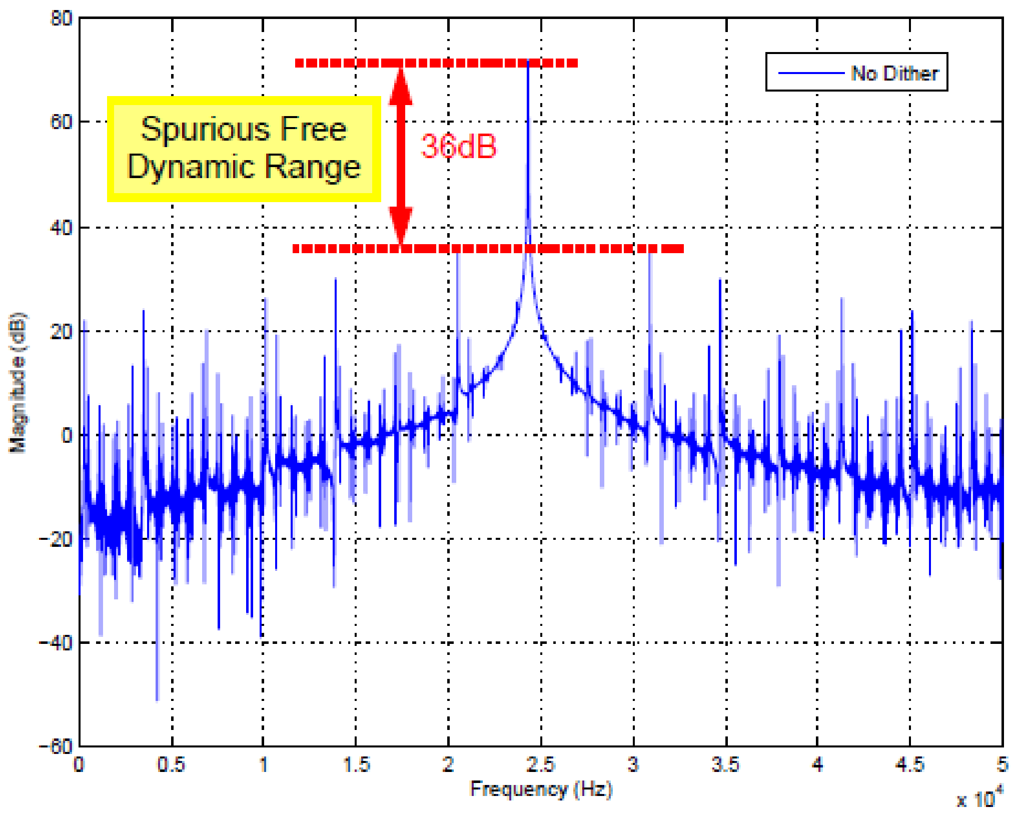
- QAUNTIZATION ERROR, small L
- fs: 100kHz, fd: 24.3kHz, **L:8**, [n:b]=[**12**:16]





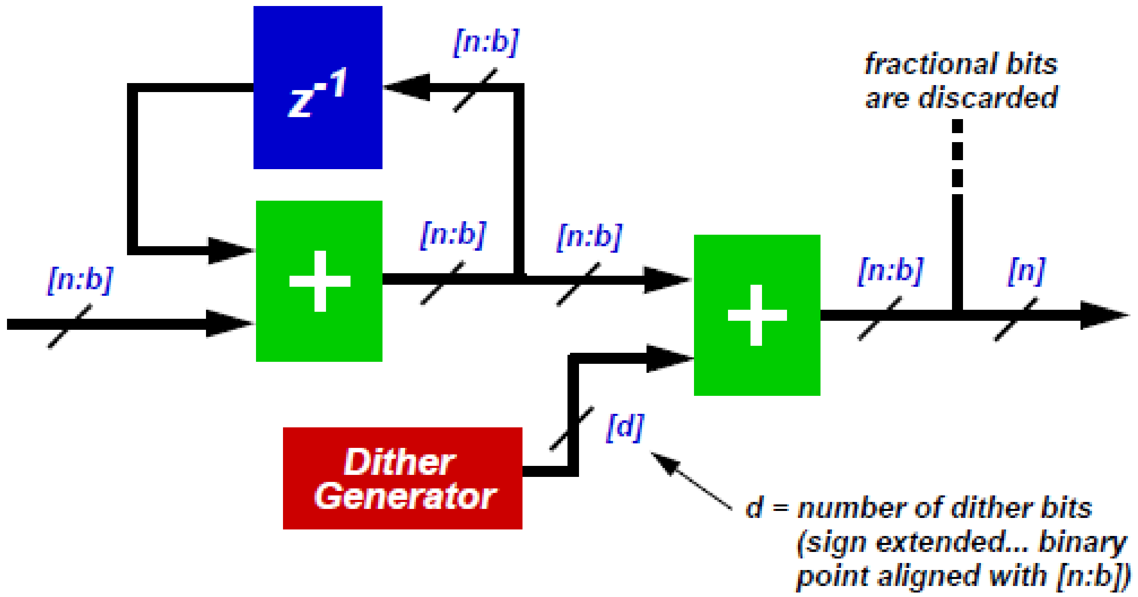
# NCO ON FPGA

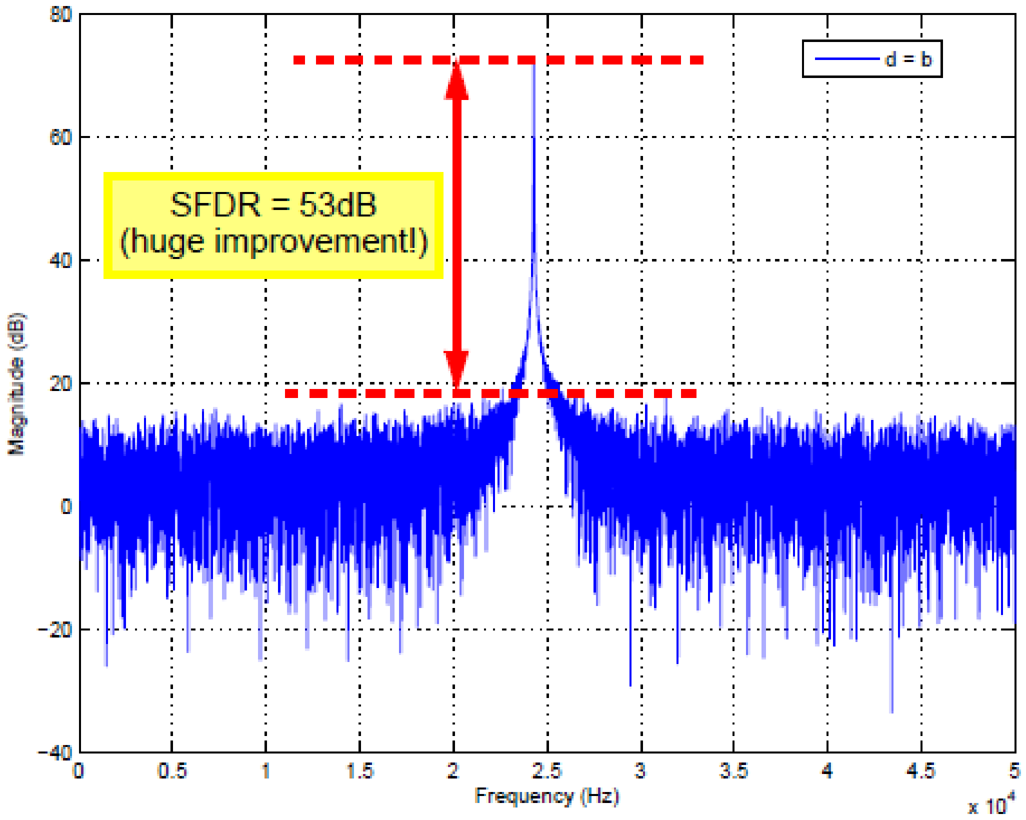
- SFDR: Range free of spurious frequencies
- GSM requires 110Db of SFDR



# NCO ON FPGA

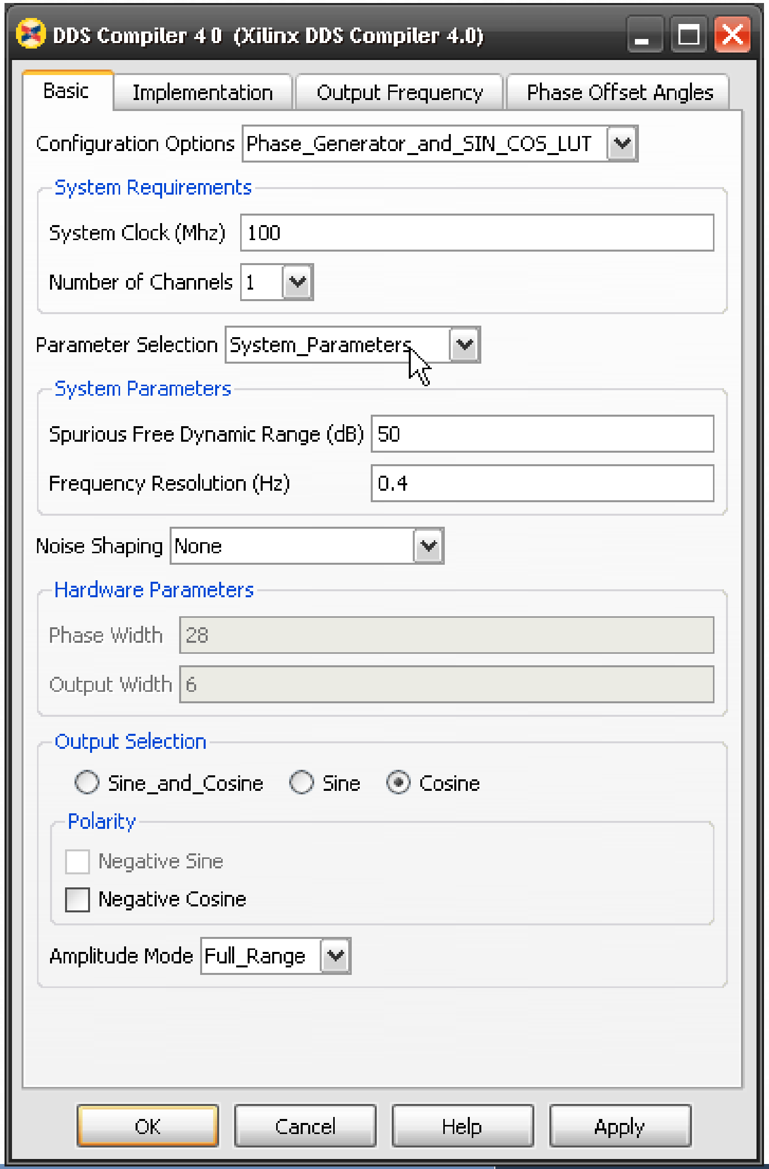
- Increase LUT size N help, but **cost a lot.**
- Better solution: add a dither signal to **break the quantization error.**
- Usually the number of dither bits is equal to fractional bits, **b=d**


z-1
[n:b]
+
[n:b]
[n:b]
[n:b]
+
[n:b]
[n]
fractional bits are discarded
Dither Generator
[d]
d = number of dither bits (sign extended... binary point aligned with [n:b])



# NCO ON FPGA

- DIRECT DIGITAL SYNTHESIZER



DDS Compiler 4.0 (Xilinx DDS Compiler 4.0)

Configuration Options: Phase_Generator_and_SIN_COS_LUT

System Requirements

System Clock (Mhz): 100

Number of Channels: 1

Parameter Selection: System_Parameters

System Parameters

Spurious Free Dynamic Range (dB): 50

Frequency Resolution (Hz): 0.4

Noise Shaping: None

Hardware Parameters

Phase Width: 28

Output Width: 6

Output Selection

○ Sine_and_Cosine ○ Sine ● Cosine

Polarity

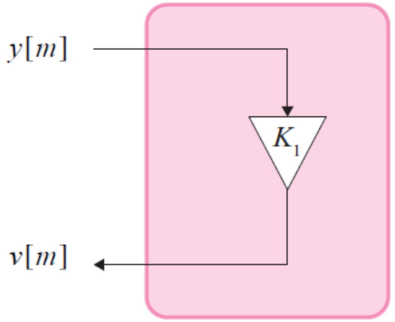
□ Negative Sine

□ Negative Cosine

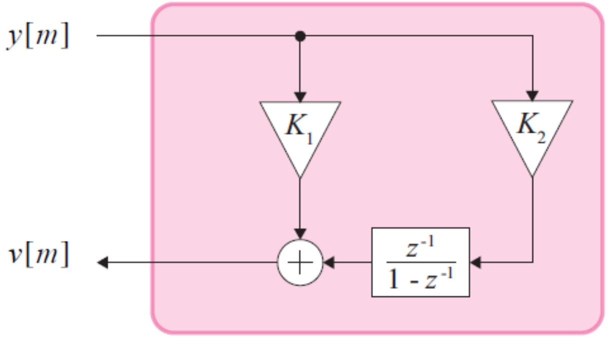
Amplitude Mode: Full_Range

# LOOP FILTERS TYPES

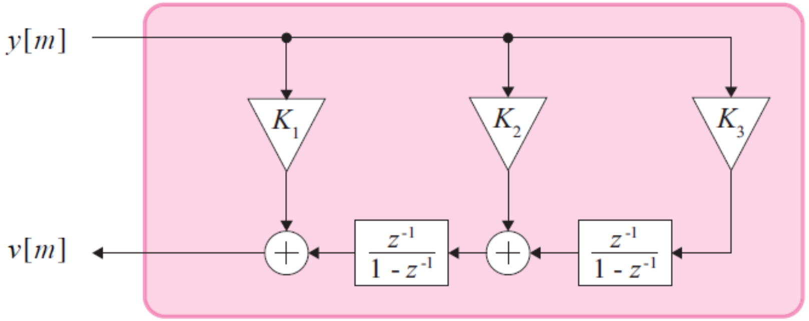
*Type 1 Loop Filter*

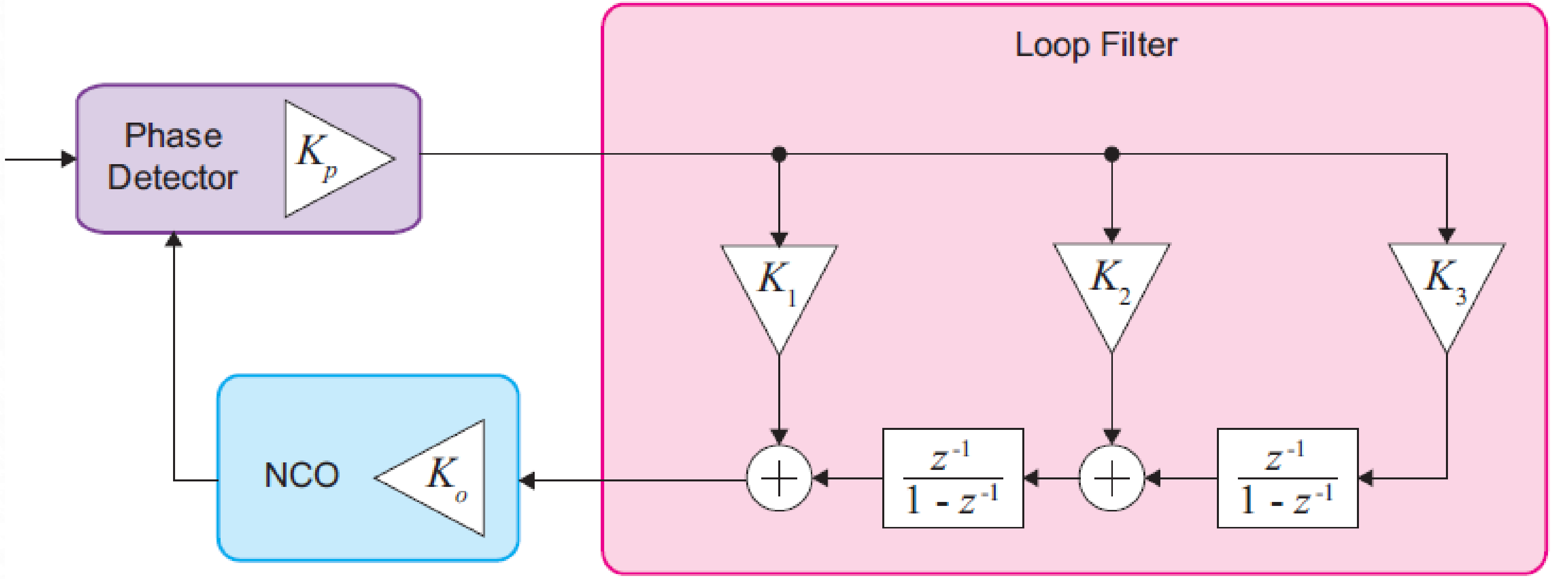


*Type 2 Loop Filter*



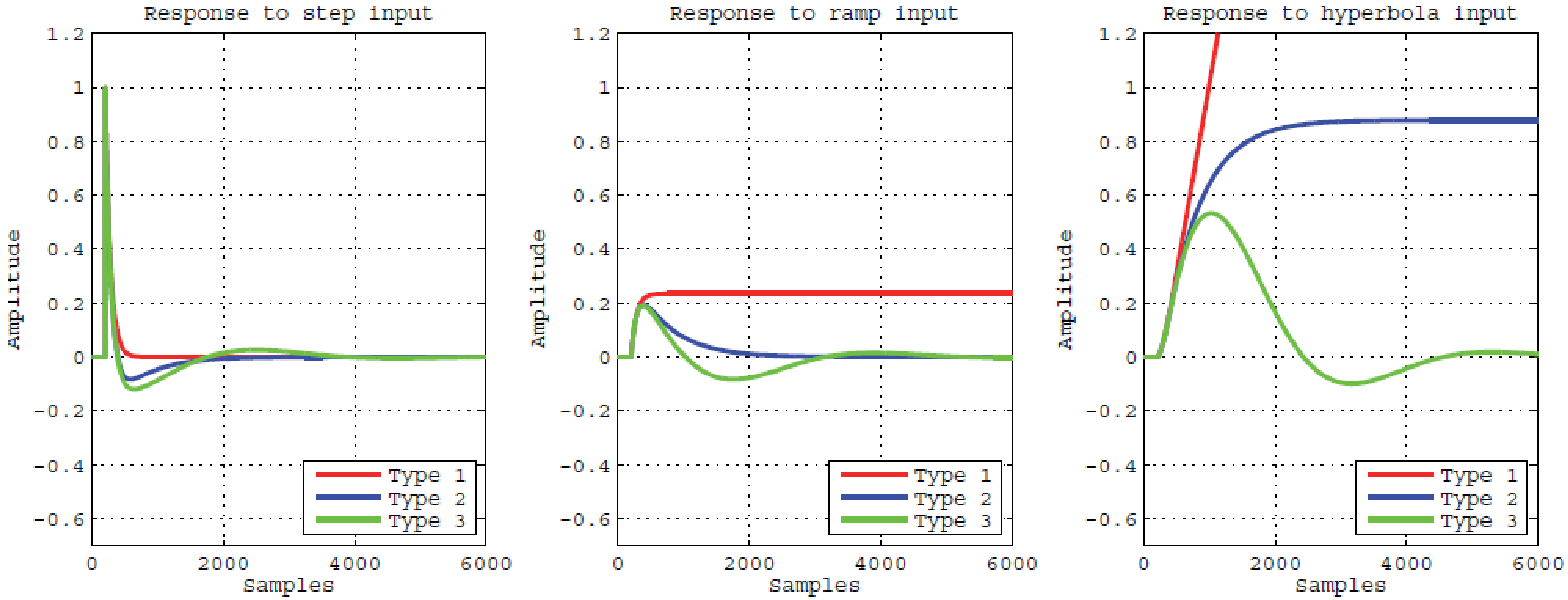
*Type 3 Loop Filter*





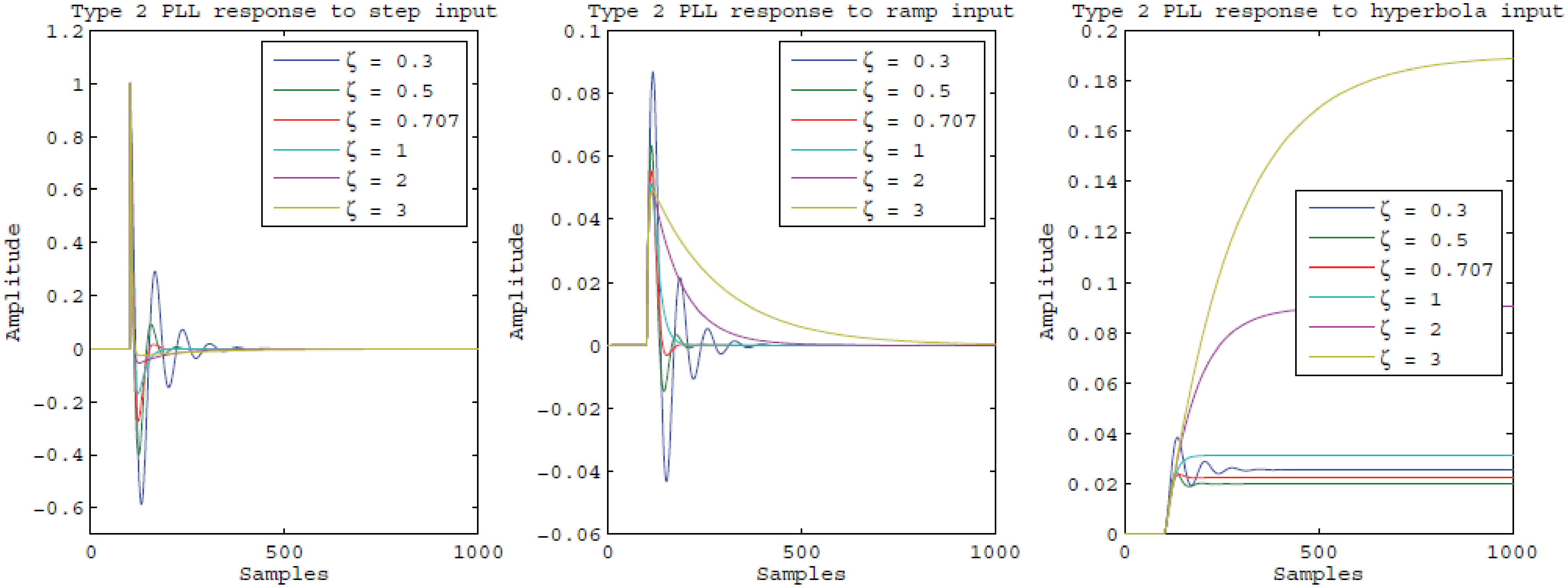
# DESIGN PARAMETERS

- Time to achieve lock, depends on the step size.
- Steady state error, depends on the number of integrators and how the input signal change.
- Tracking capabilities, deepens on the PLL type.



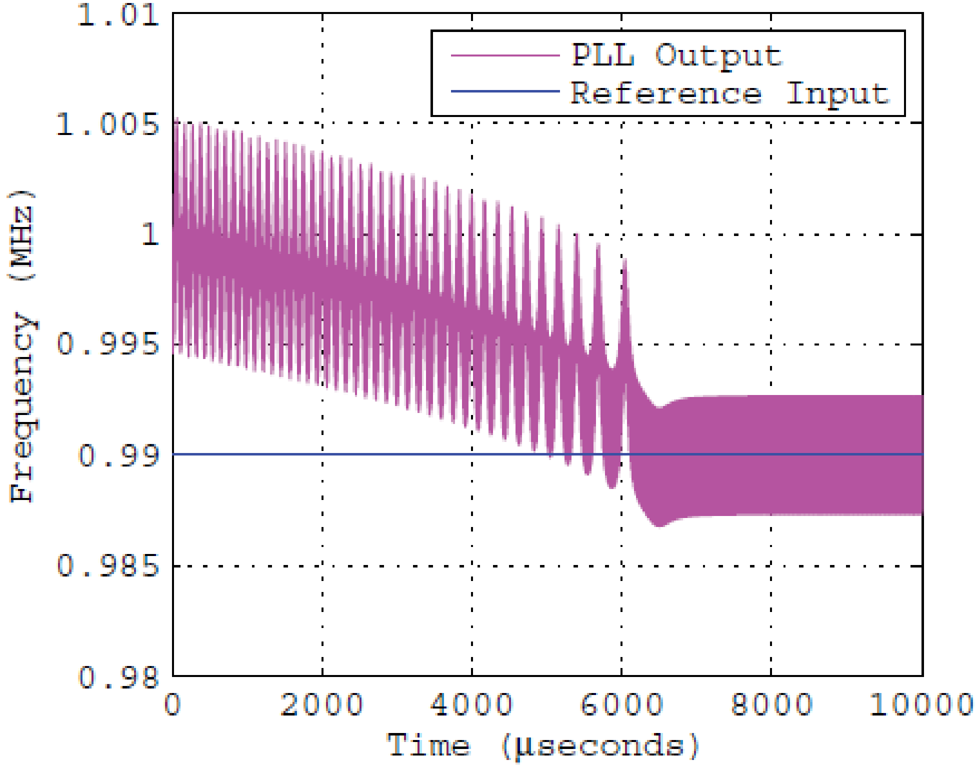
# DAMPING RATIO

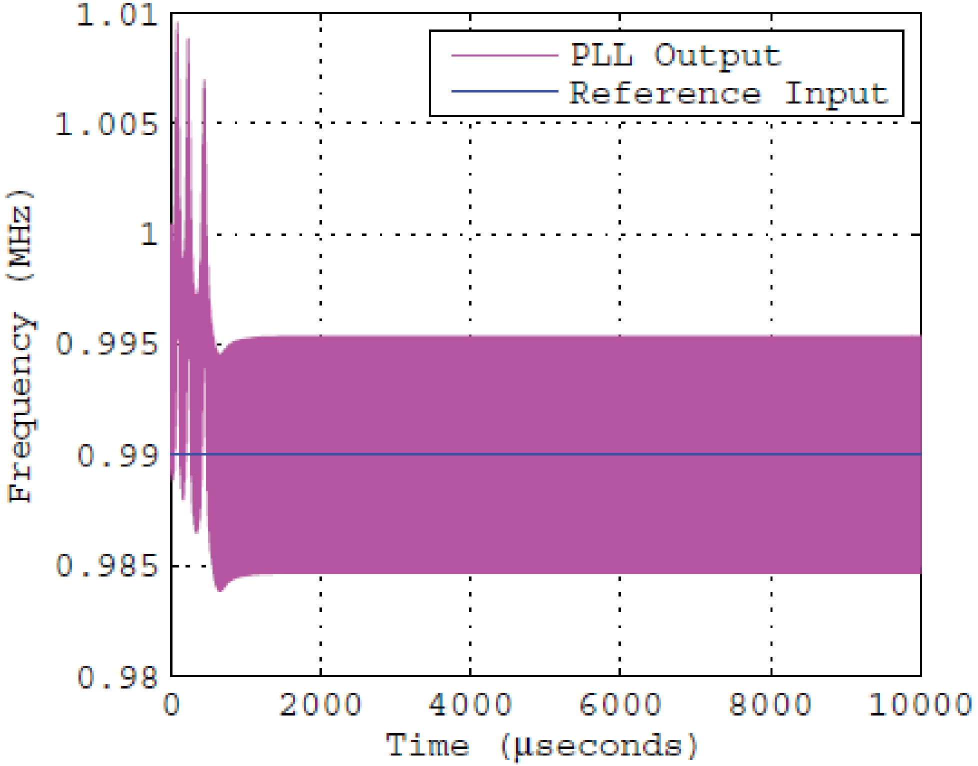
- $\zeta < 1$ under-damped $\zeta > 1$ over damped $\zeta = 1$ critically damped
- The damping factor, or damping *ratio*, relates to the transient behavior of the PLL as it achieves phase lock.
- Typical value is *0,707*



# BANDWIDTH

- The bandwidth refers to the range of frequencies over which the PLL operates
- At lower BW, bigger transient time at bigger BW lower transient. Cons: more noise into the PLL.

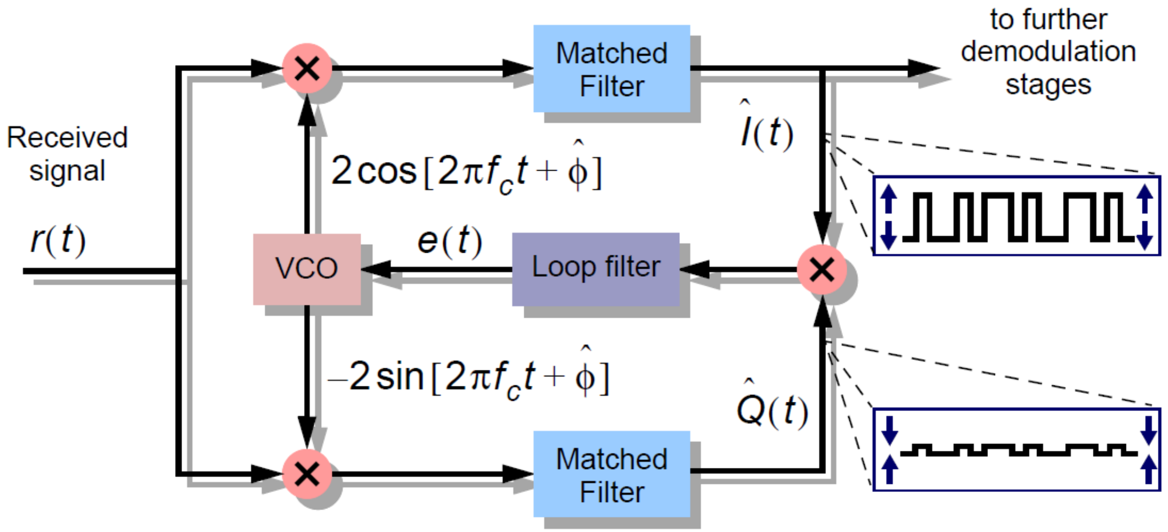




# COSTAS LOOP

- It is a type of PLL used on AM-DSB-SC demodulation. Also used on M-PSK demodulations.
- It is based on the sin vs cos orthogonality.
- Principal advantage is its double sensibility . **sen($\boldsymbol{2(\theta i - \theta f)}$)**
- Especially useful for Doppler effect correction.

$$r(t) = A(t)\cos(2\pi f_c t + \phi)$$


Received signal
$r(t)$
Matched Filter
to further demodulation stages
$\hat{I}(t)$
$2\cos[2\pi f_c t + \hat{\phi}]$
VCO
$e(t)$
Loop filter
$-2\sin[2\pi f_c t + \hat{\phi}]$
$\hat{Q}(t)$
Matched Filter

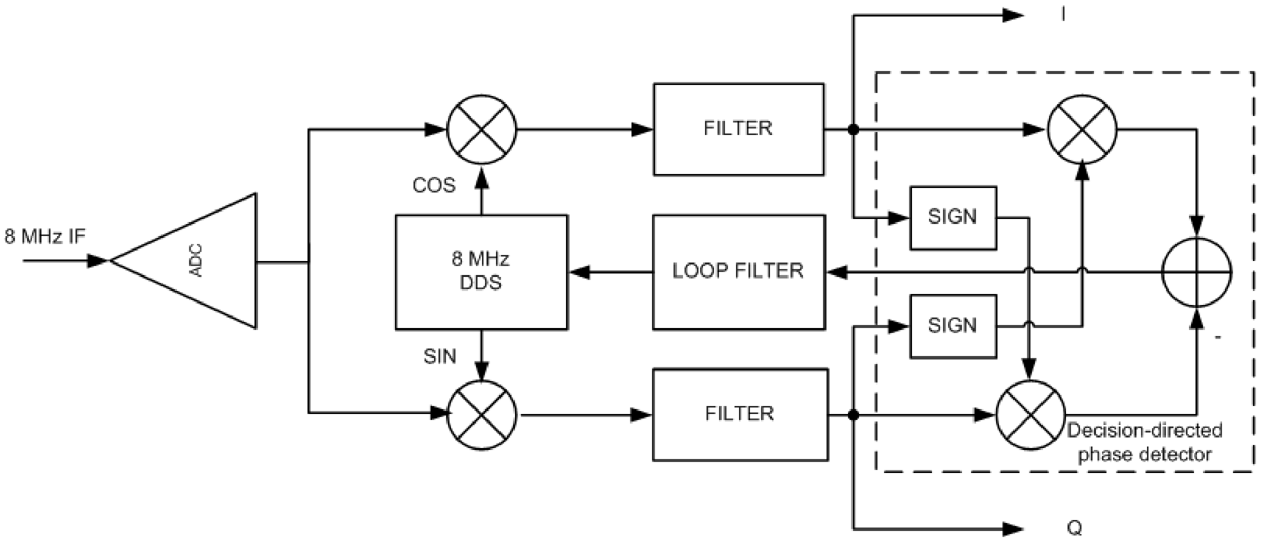
$$\hat{I}(t) = A(t)\cos(\phi - \hat{\phi})$$

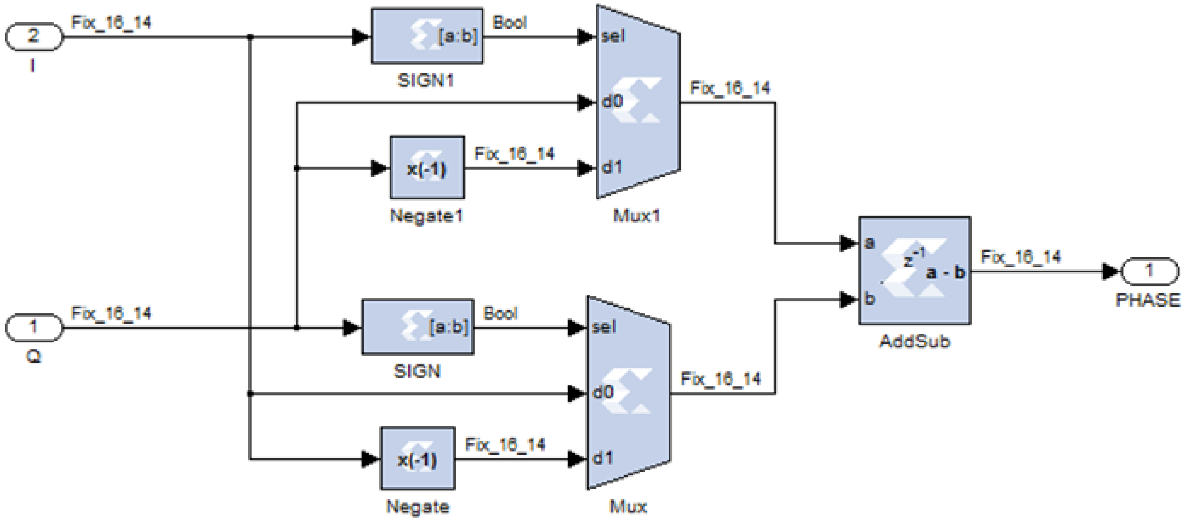
$$\hat{Q}(t) = A(t)\sin(\phi - \hat{\phi})$$

$$\begin{aligned} e(t) &= A^2(t)\cos(\phi - \hat{\phi})\sin(\phi - \hat{\phi}) \\ &= \frac{1}{2}A^2(t)\sin(2(\phi - \hat{\phi})) \end{aligned}$$

# COSTAS LOOP FPGA IMPLEMENTATION

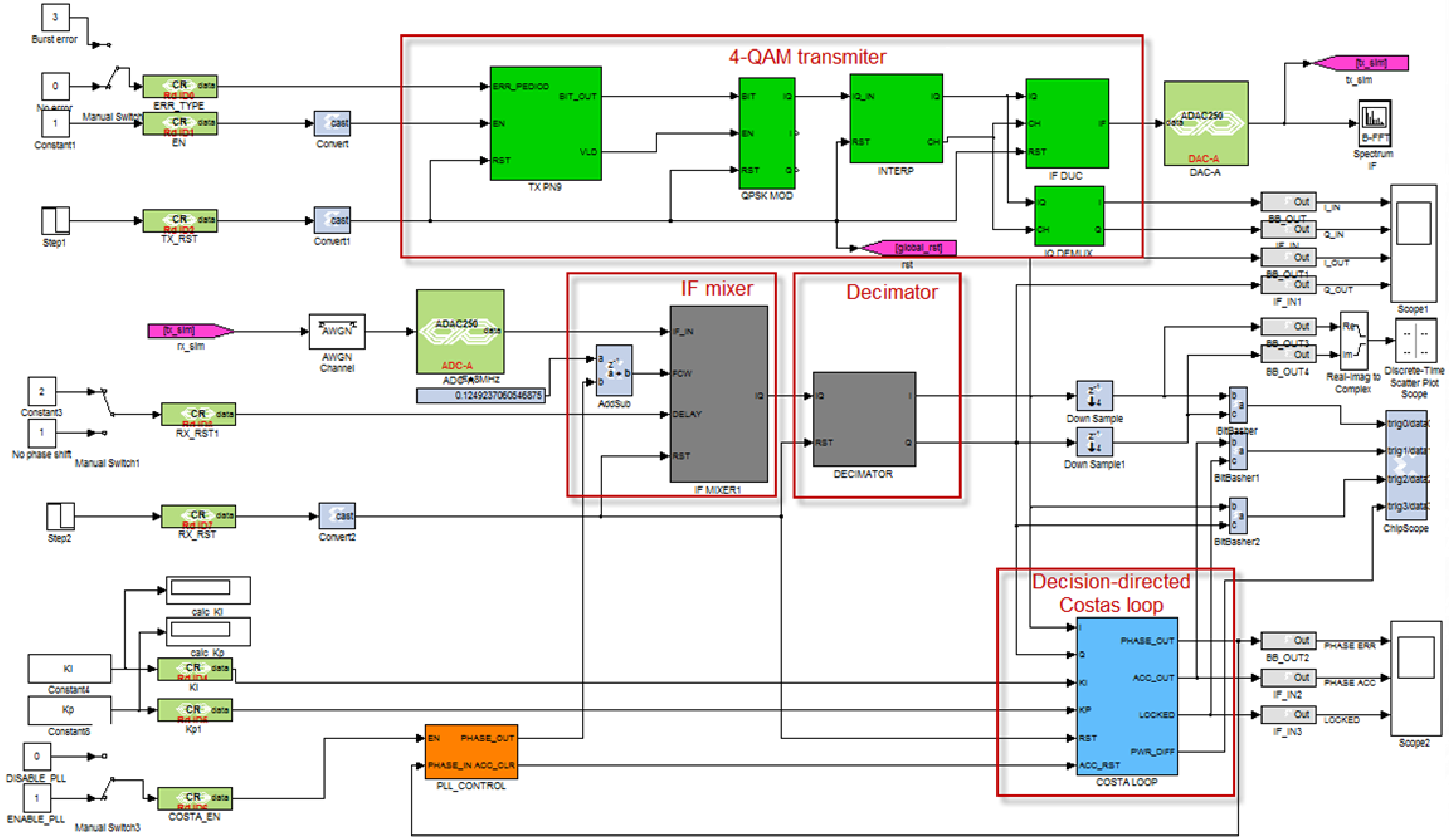
- Decision Direct PLL





# COSTAS LOOP EXAMPLE

- 4QAM RX/TX


4-QAM transmiter
IF mixer
Decimator
Decision-directed Costas loop
Burst error
No error
Constant1
Manual Switch
ERR_TYPE
EN
Step1
TX_RST
Convert
Convert1
TX PN9
ERR_PEDIOD
BIT_OUT
VLD
RST
QPSK MOD
INTERP
IF DUC
IQ DEMUX
[global_rst]
rst
ADAC250
DAC-A
[tx_sim]
tx_sim
B-FFT
Spectrum IF
BB_OUT
IF_IN
BB_OUT1
IF_IN1
I_IN
Q_IN
I_OUT
Q_OUT
Scope1
BB_OUT3
BB_OUT4
Real-Imag to Complex
Discrete-Time Scatter Plot Scope
rx_sim
AWGN Channel
ADC-A
0.1249237060546875
Constant3
No phase shift
Manual Switch1
RX_RST1
Step2
RX_RST
Convert2
AddSub
IF MIXER1
IF_IN
POW
DELAY
DECIMATOR
Down Sample
Down Sample1
BitBasher
BitBasher1
BitBasher2
ChipScope
trig0/data
trig1/data
trig2/data
trig3/data
calc KI
calc Kp
KI
Kp
Constant4
Constant5
Kp1
DISABLE_PLL
ENABLE_PLL
Manual Switch3
COSTA_EN
PLL_CONTROL
PHASE_OUT
PHASE_IN
ACC_CLR
COSTA LOOP
PHASE_OUT
ACC_OUT
LOCKED
PWR_DIFF
ACC_RST
BB_OUT2
IF_IN2
IF_IN3
PHASE ERR
PHASE ACC
LOCKED
Scope2